



# H55H-CM

V : 1.0


## SCHEMATICS TABLE:

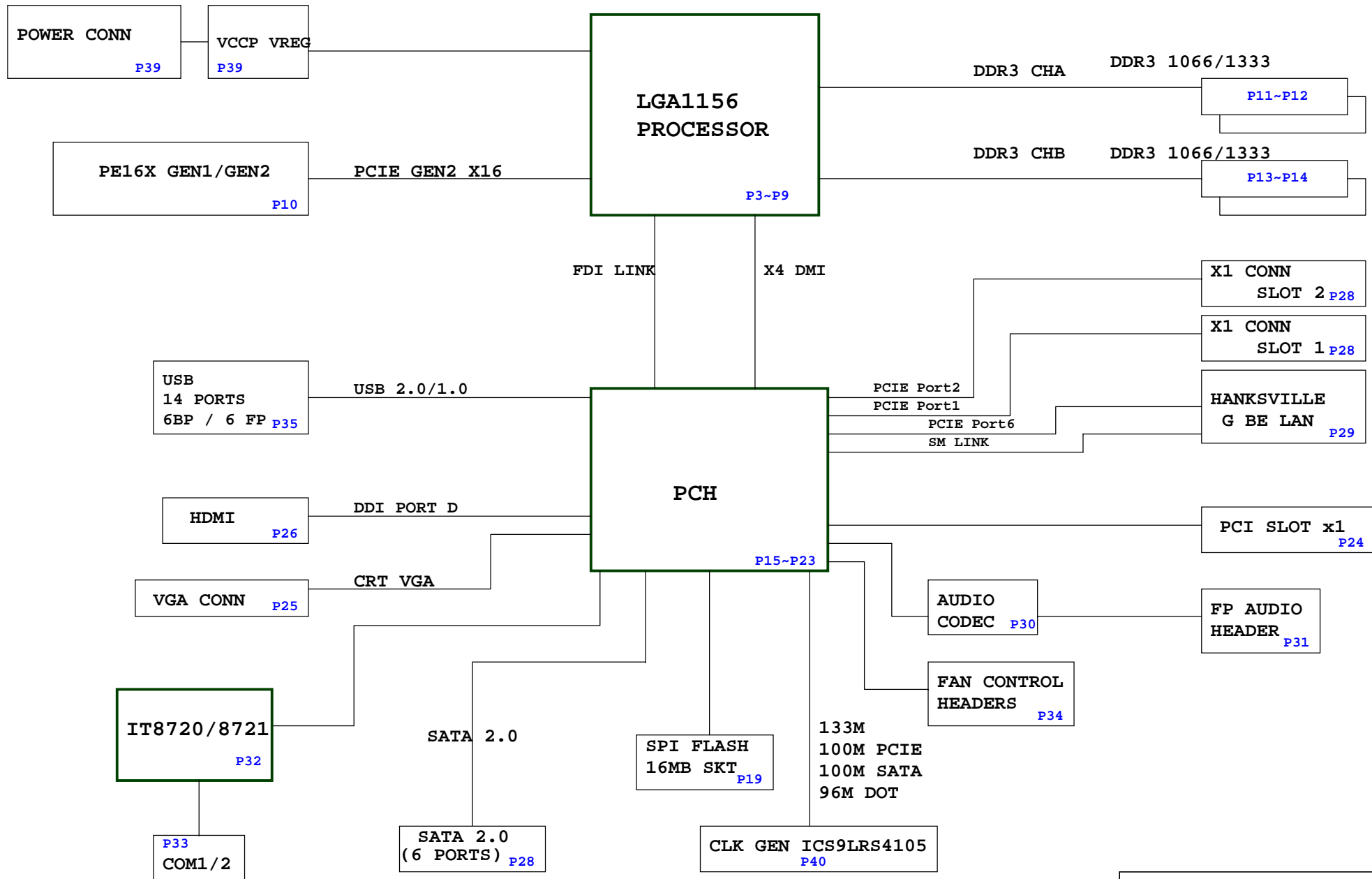
Page	Index	Page	Index
1	COVER PAGE	24	PCI
2	Block Diagram	25	VGA Connector
3	CPU MISC&Flexible Display Interface	26	HDMI(Level shifter&Connector)
4	CPU DMI&PEG	27	Primary&PCH XDP
5	CPU DDR3-A	28	SATA&PCI-E X1
6	CPU DDR3-B	29	Hanksville(82578DC)
7	CPU CFG	30	Audio ALC662/ALC888S
8	CPU Power(VCCP,V_AXG,VTT)	31	Audio Connector
9	CPU GND&RSVD	32	IT8720F/8721F
10	PCI-E 16X	33	COM,KBMS,FDD,LPT
11	CONN DDR3 CH A DIMM0	34	F_PANEL&Smart Fan
12	CONN DDR3 CH A DIMM1	35	USB Header&Port
13	CONN DDR3 CH B DIMM0	36	DC-DC CPU_VTT,5VDUAL
14	CONN DDR3 CH B DIMM1	37	DC-DC V_AXG,V_1P05_ME
15	PCH USB&PCIE	38	DC-DC PCH Core,VDIMM,V_1P8_SFR
16	PCH SATA,HOST,CLINK,PCI	39	DC-DC CPU Vcore
17	PCH GPIO,AUDIO,LPC,SPI	40	CLK GEN CK505(ICS9LRS4105)
18	PCH NVRAM	41	Power Delivery
19	PCH FDLINK&SPI ROM&TCM	42	PWRGD&RST Tree
20	PCH PWR RAILS,Decoupling	43	Clock Map
21	PCH GND Pins		
22	PCH Video and DDSP		
23	PCH CLOCKS,Straps		

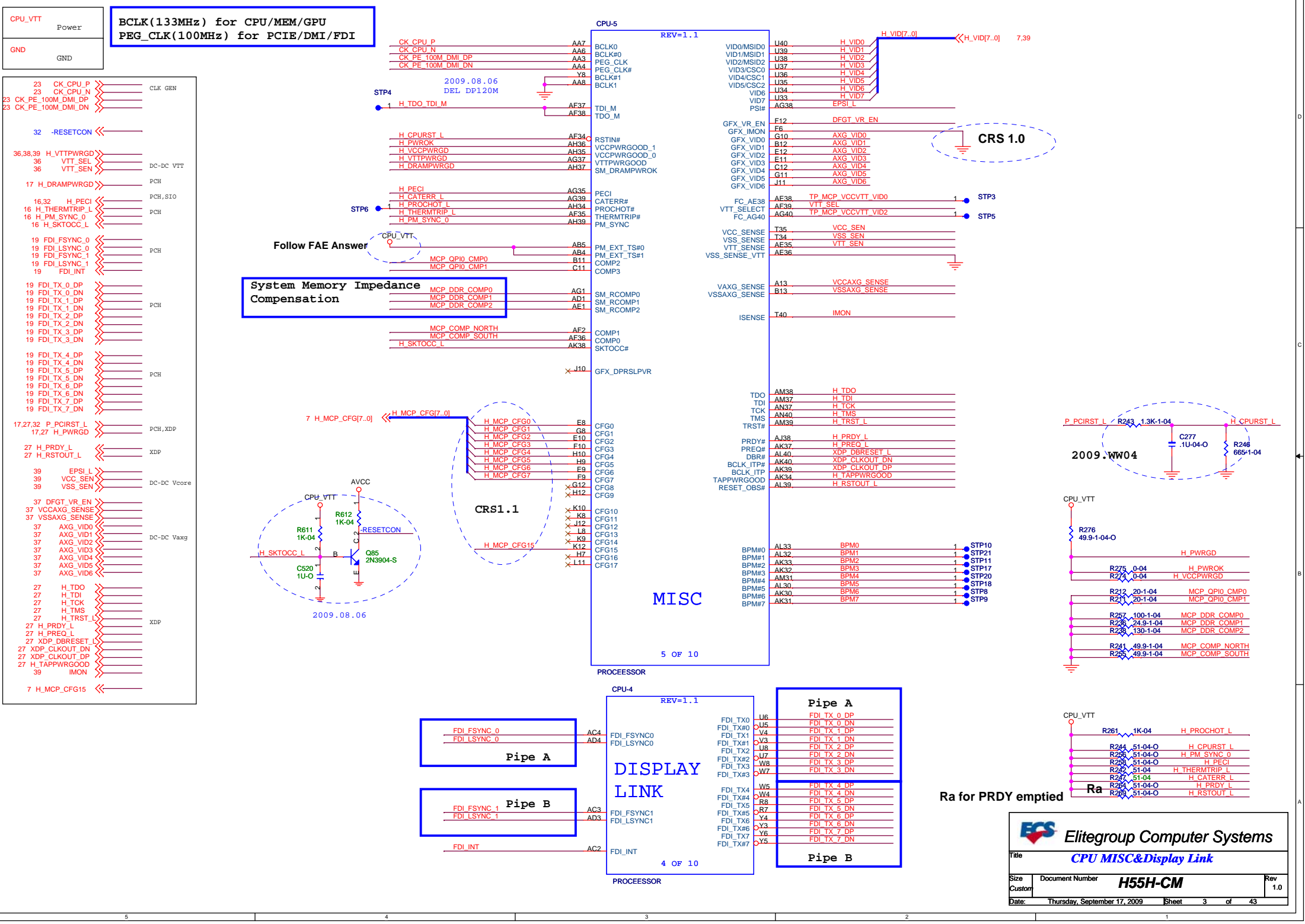
## REVISION HISTORY:

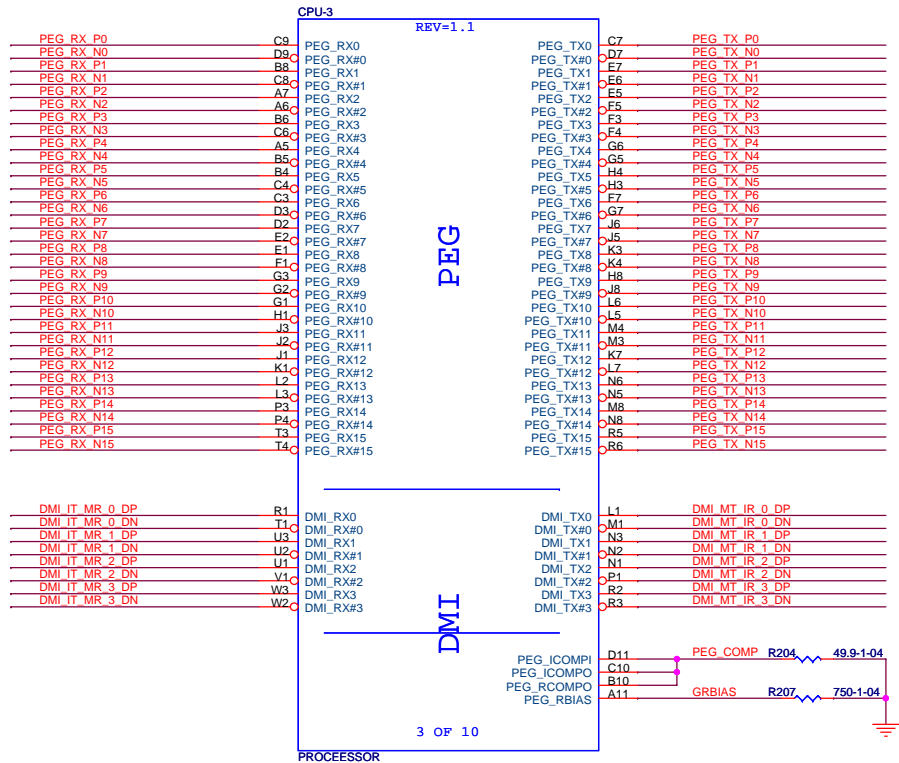
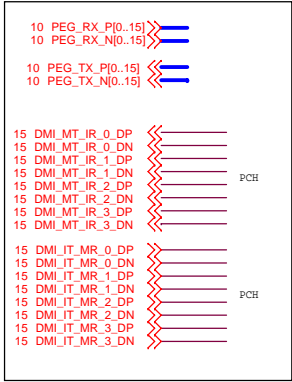
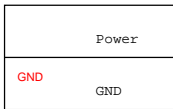
Rev	Date	Notes
V1.0	2009/10/29	1.change model name to H55H-CM 2.change PCH to H55 3.Add HDMI&VGA function

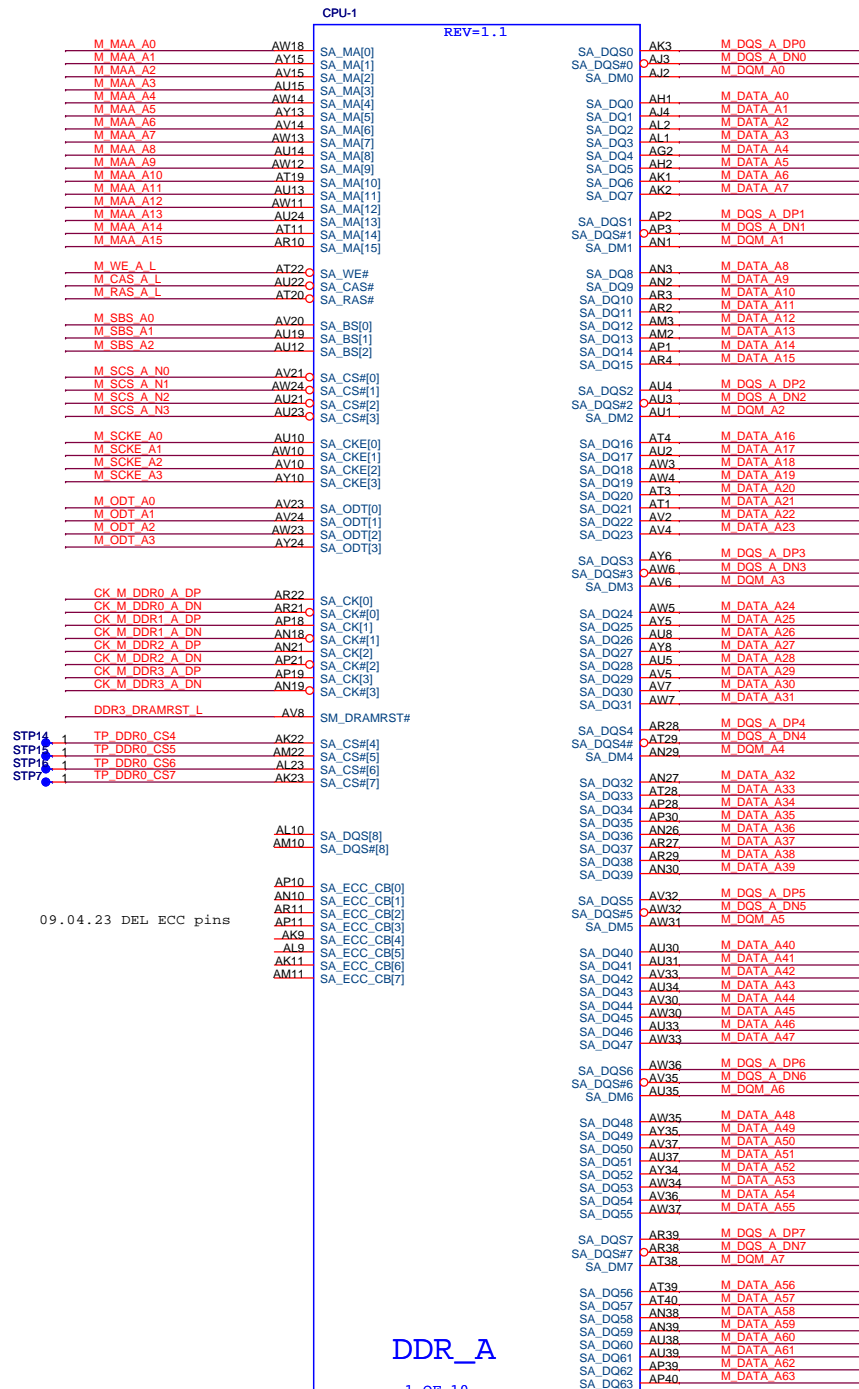
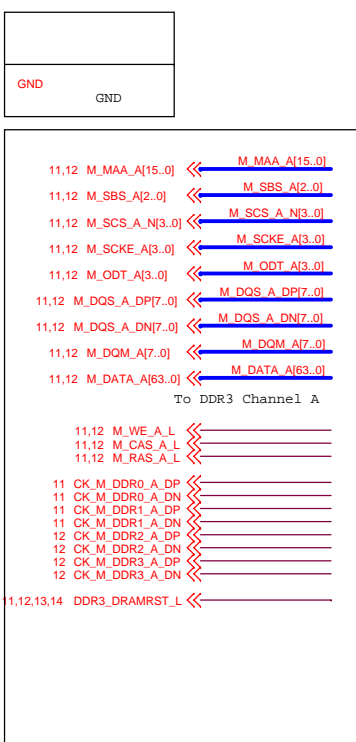
@ ECS CONFIDENTIAL @

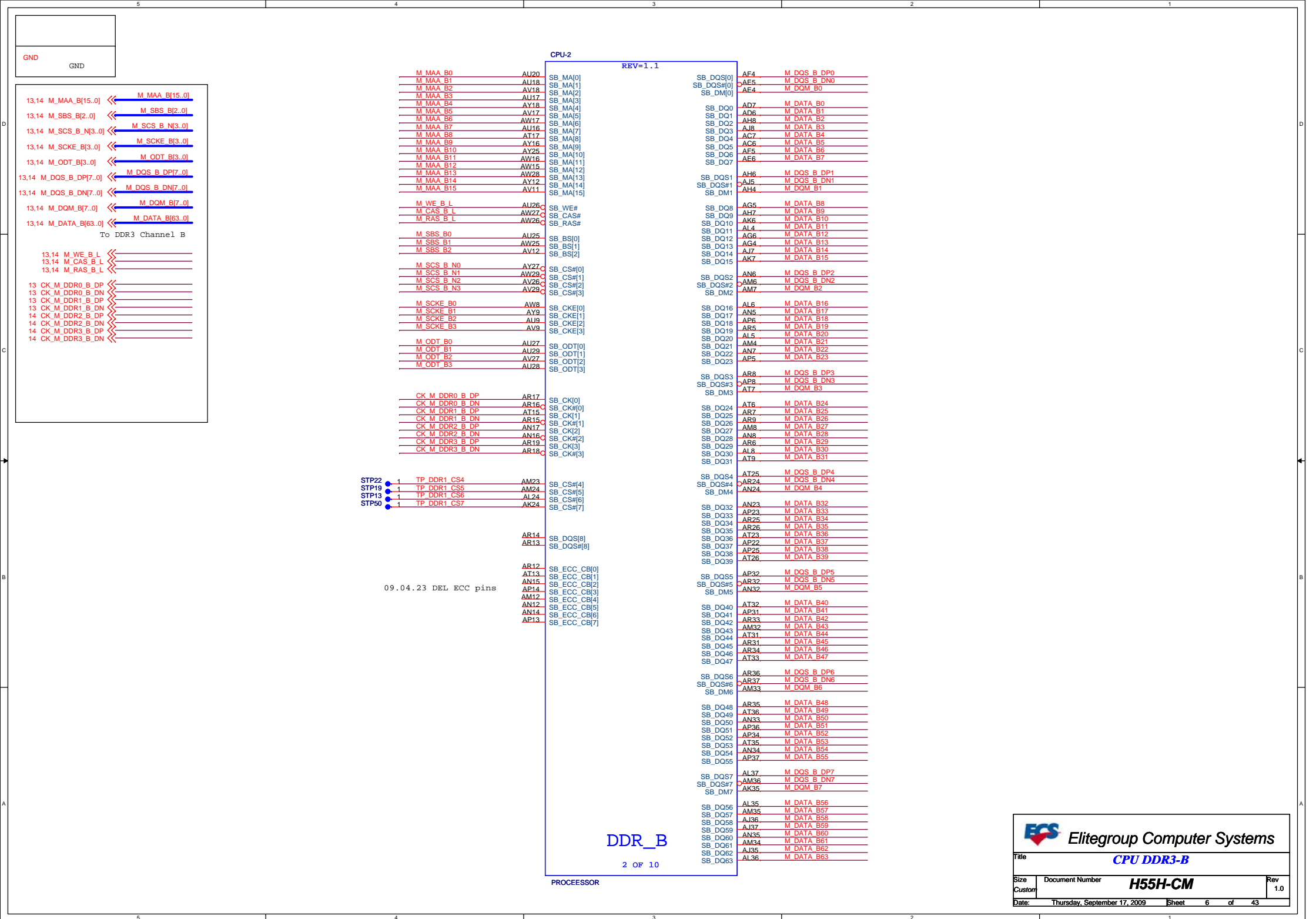
 Elitegroup Computer Systems	
Title <i>Cover Page</i>	
Size Custom	Document Number <b>H55H-CM</b> Rev 1.0
Date: Thursday, October 29, 2009	Sheet 1 of 43



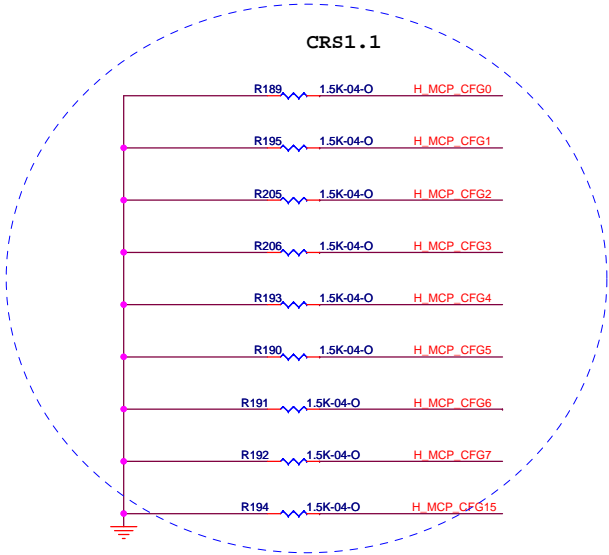
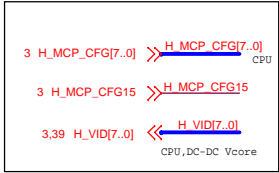




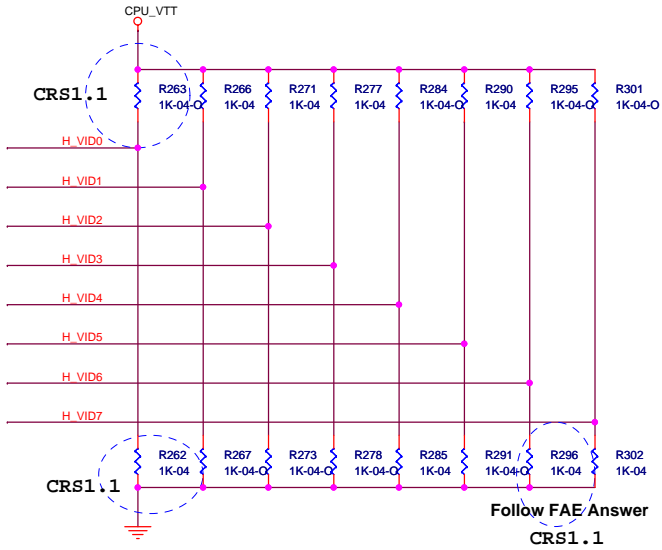




CPU_VTT	Power
GND	GND



CFG	Havendale	Lynnfield	DESCRIPTION
0	1X16	2X8	PEG SEL (1X16, 2X8)
1	RSVD		PEG SEL1
2	RSVD		PEG SEL3
3	NORM	REVERSED	PEG LANE REVERSAL
4	DISABLED	ENABLED	DP PRESENCE
	RSVD		
6	RSVD		
7	RSVD		ENGINEERING - REMOVE ON PRODUCTION DESIGN
15	RSVD		ENGINEERING - REMOVE ON PRODUCTION DESIGN
CFG 0,1,2,3,4,5,6,7,15 HAVE INTERNAL PULL-UPS			



POWER ON CONFIGURATION (POC)TABLE

	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1		
VID3	IMON CONFIG0	1	lcc(MAX)=120A	lcc(MAX)=120A
VID4	IMON CONFIG1	0		
VID5	IMON CONFIG2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

Title

CPU CFG

Size

Document Number

H55H-CM

Rev

1.0

Date:

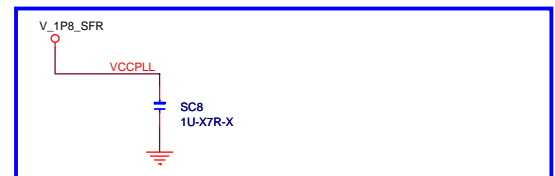
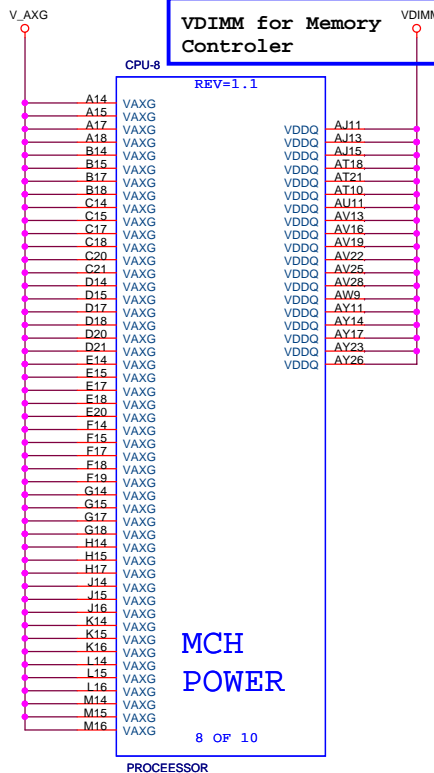
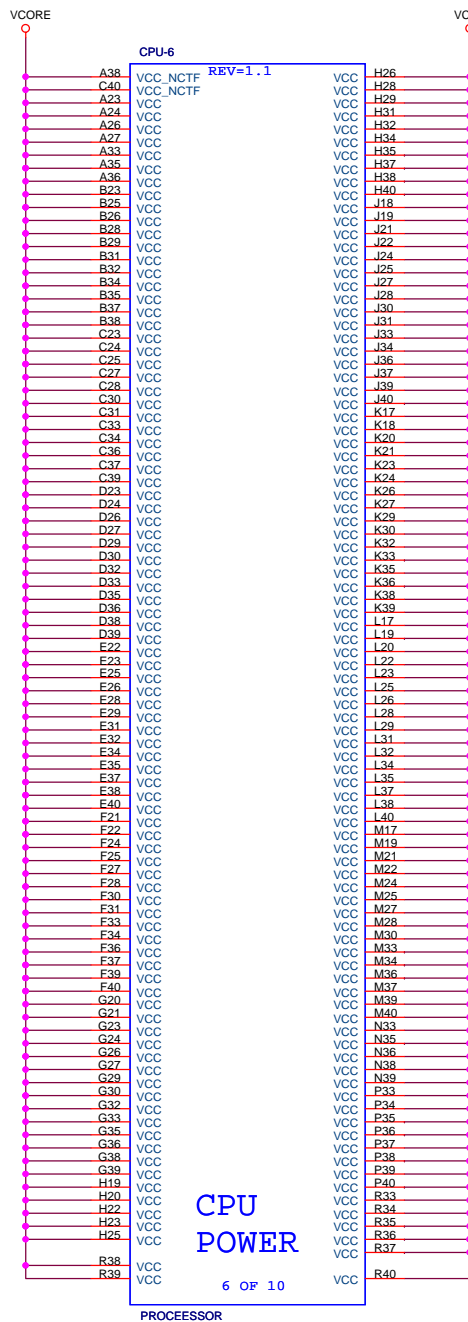
Thursday, September 17, 2009

Sheet

7

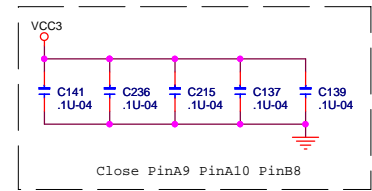
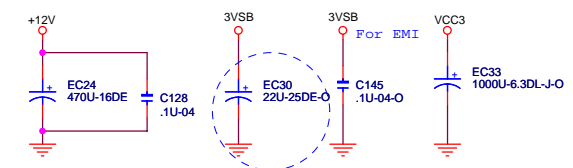
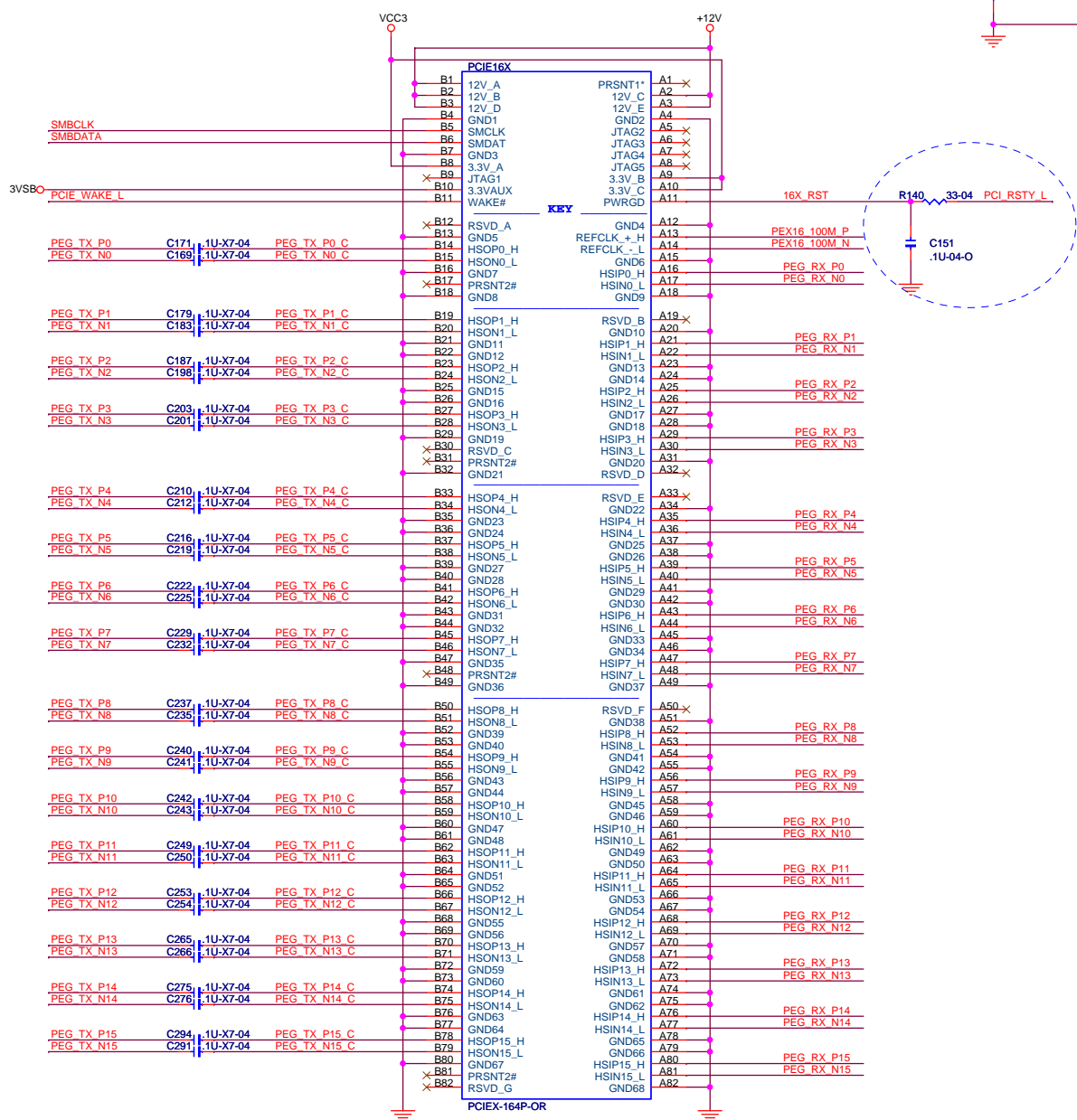
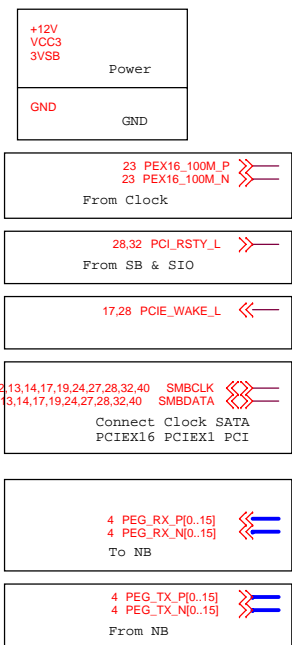
of

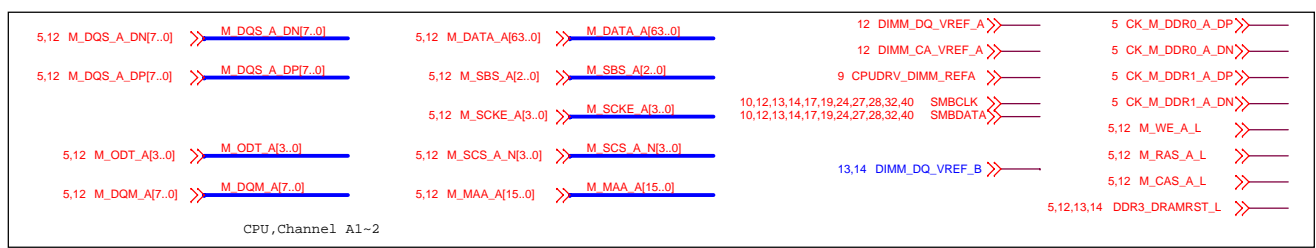
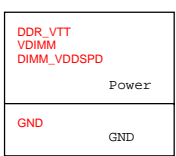
43



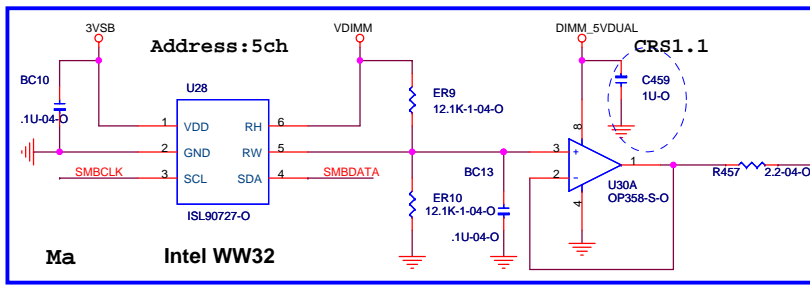
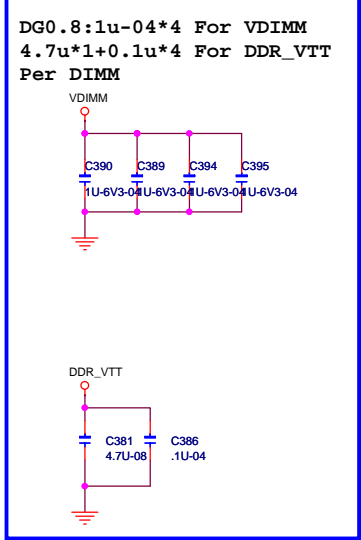
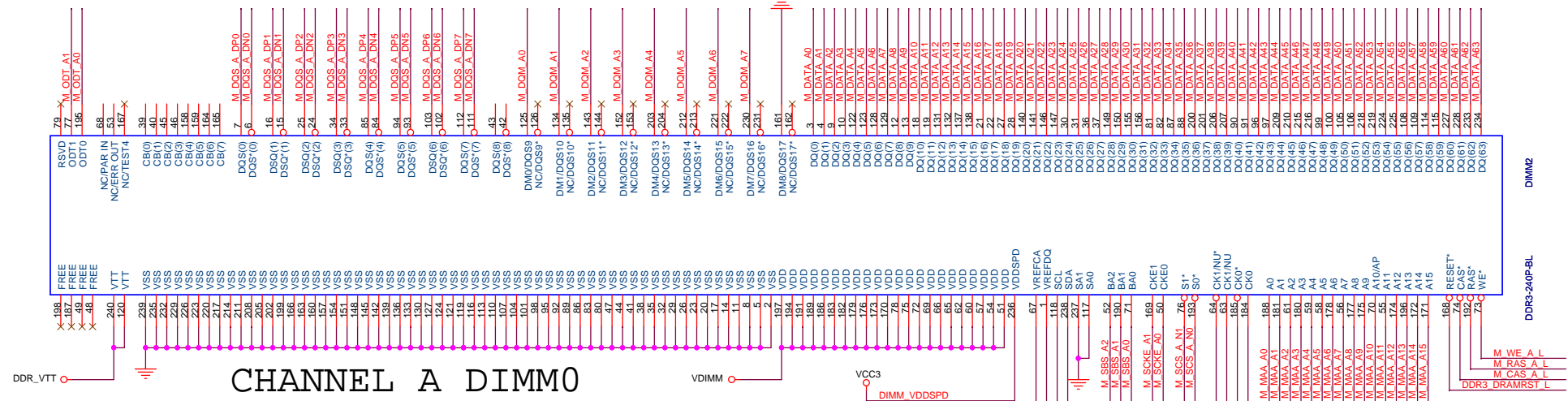




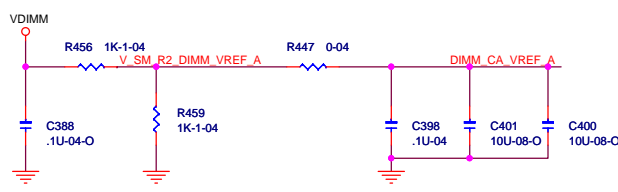
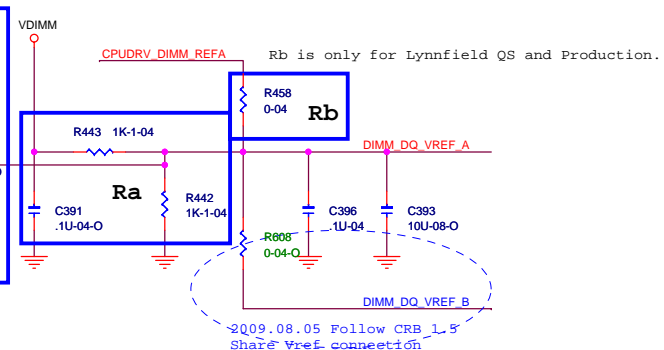


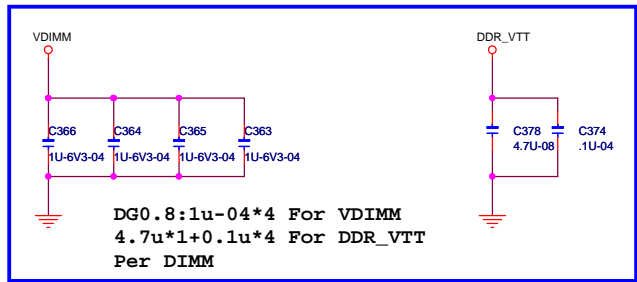
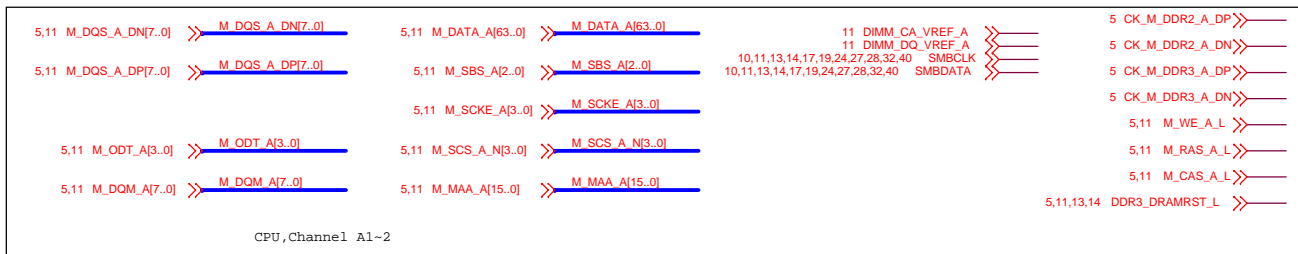


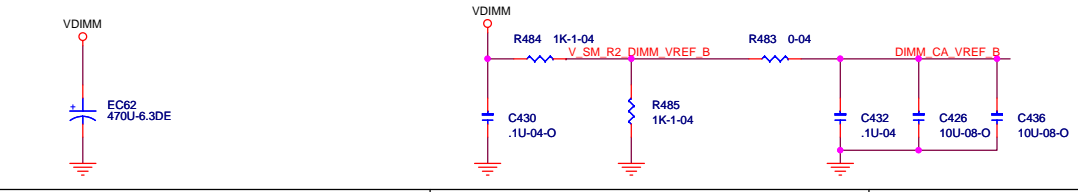
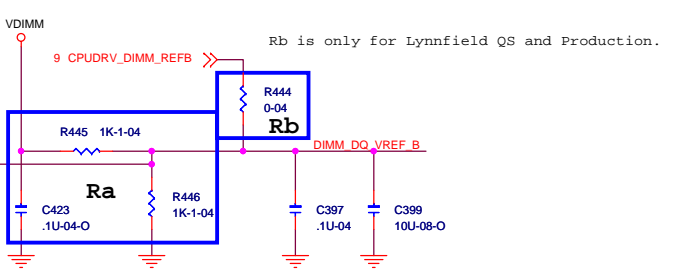
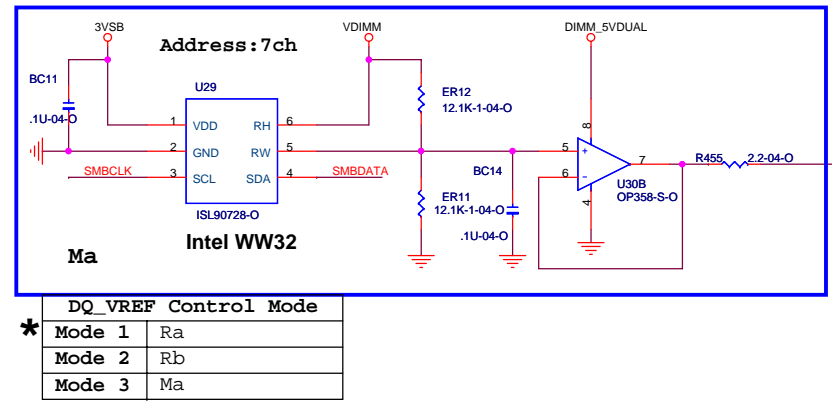
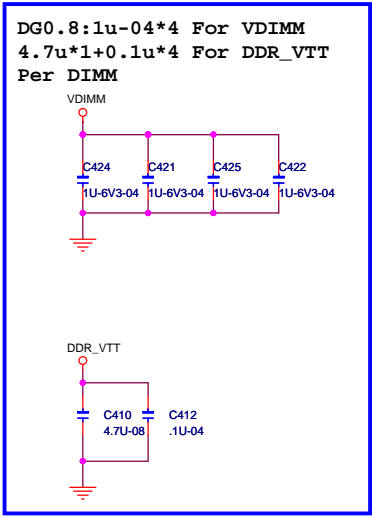
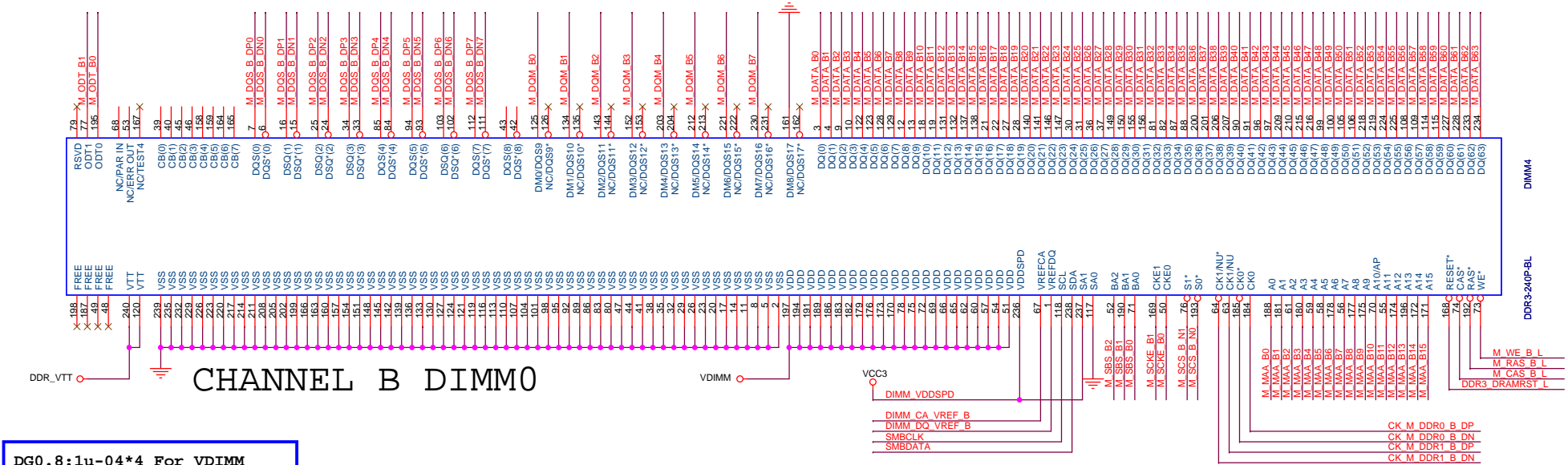
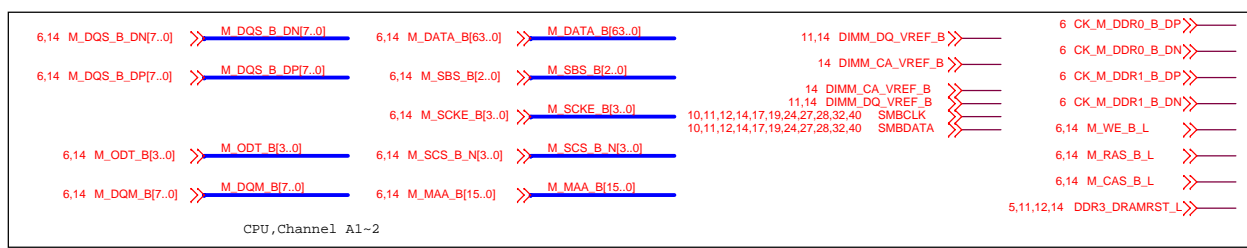
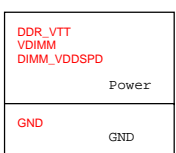
CPU,Channel A1-2

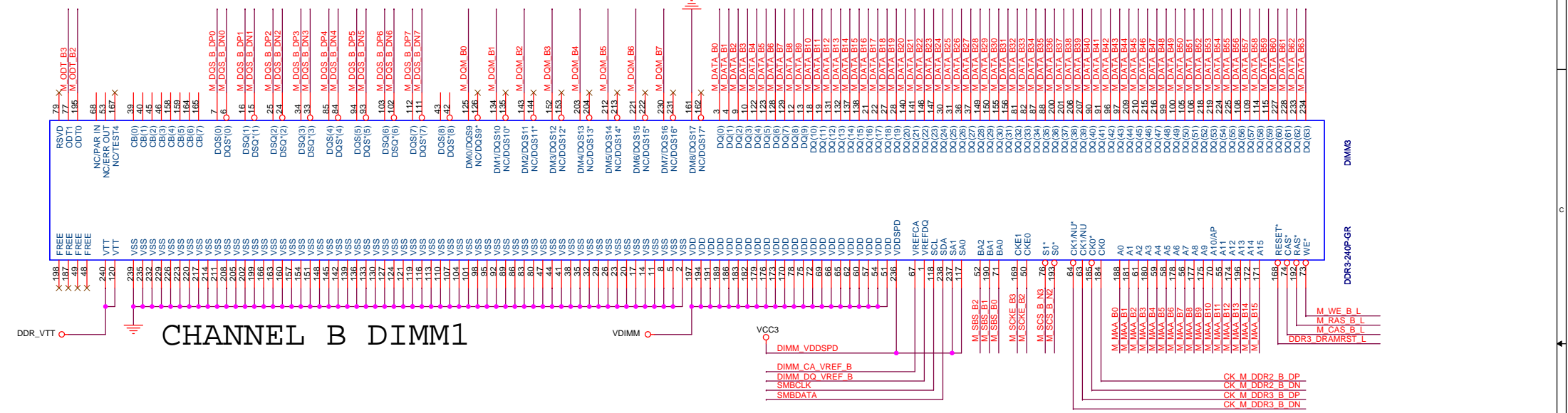
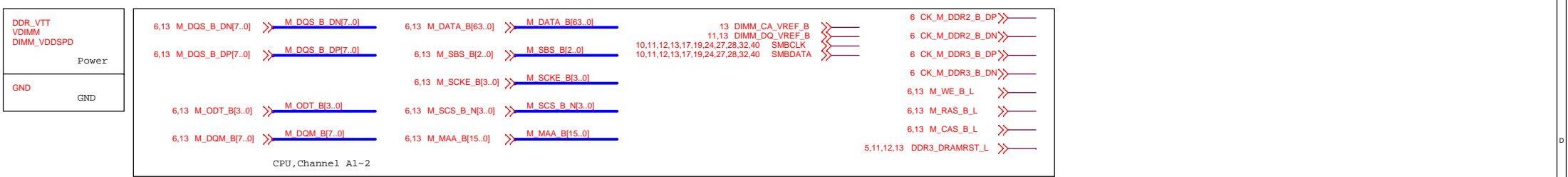


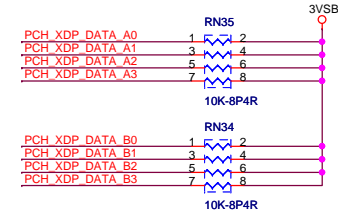
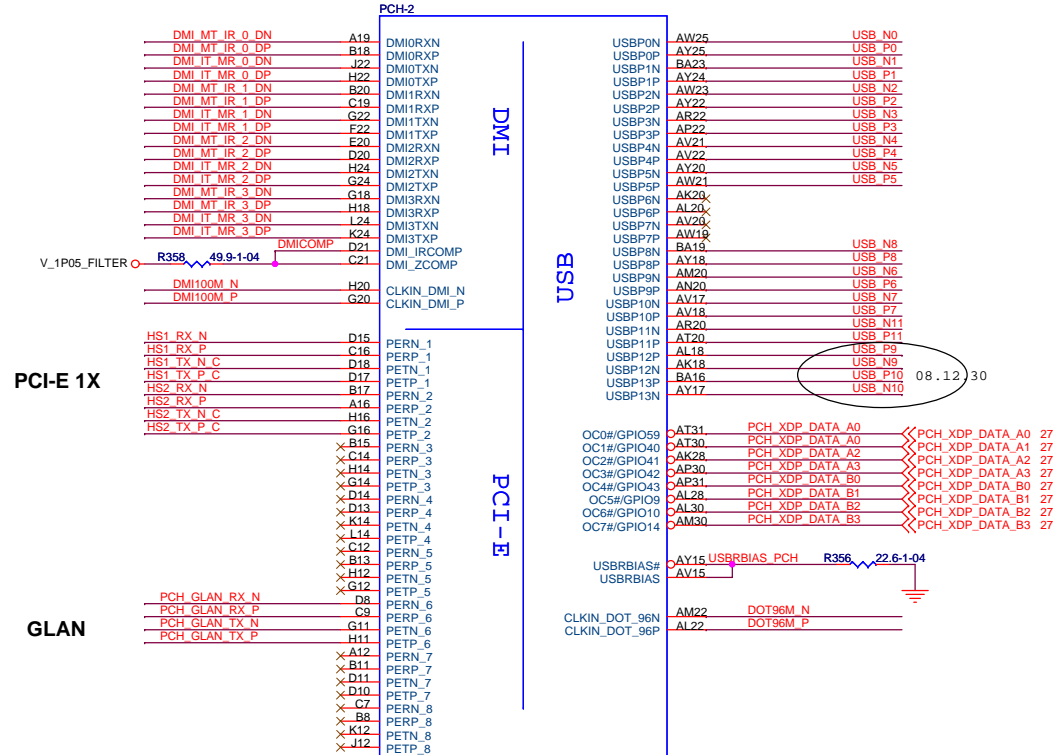
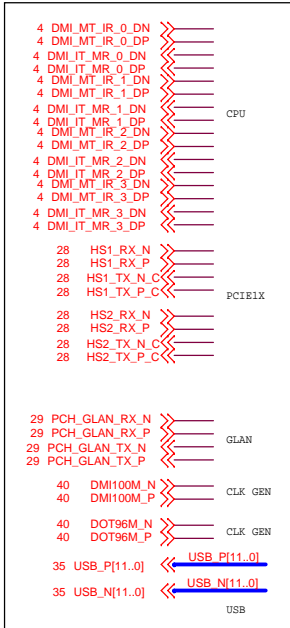
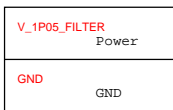
DQ_VREF Control Mode	
Mode 1	Ra
Mode 2	Rb
Mode 3	Ma

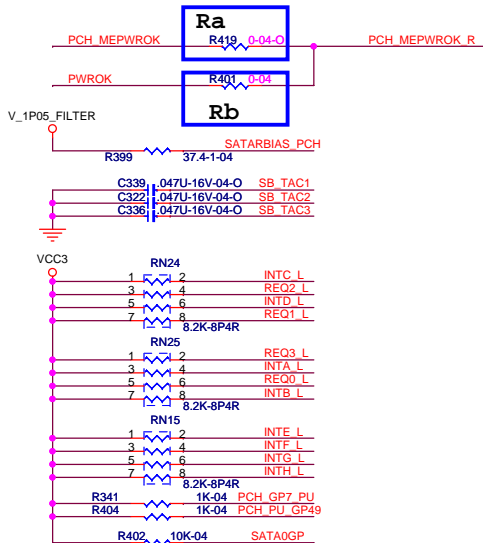
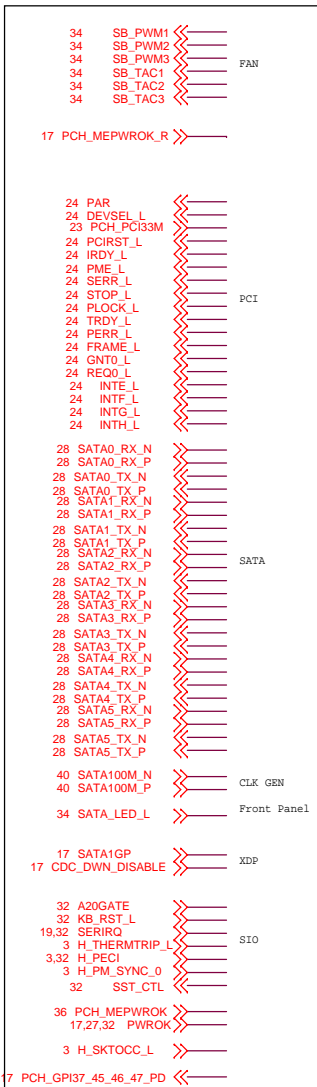
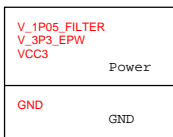




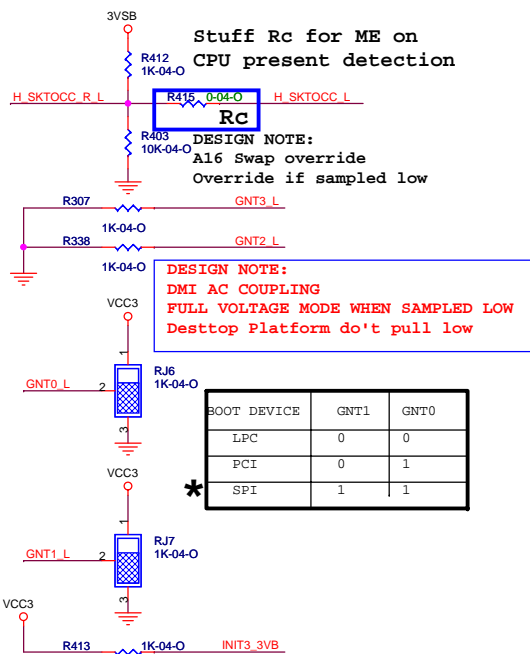
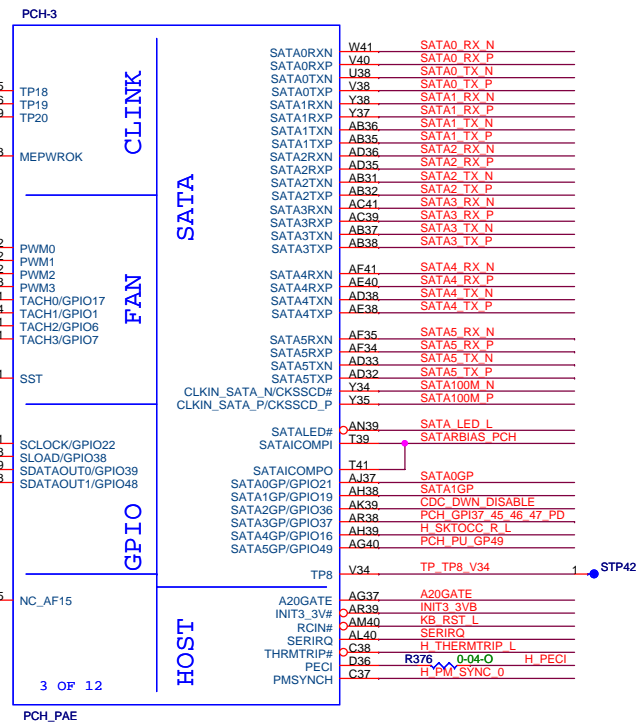
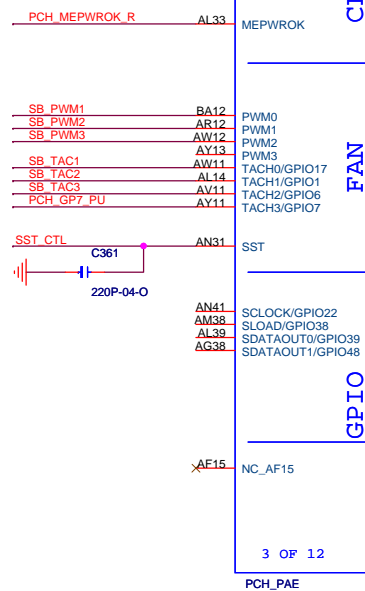




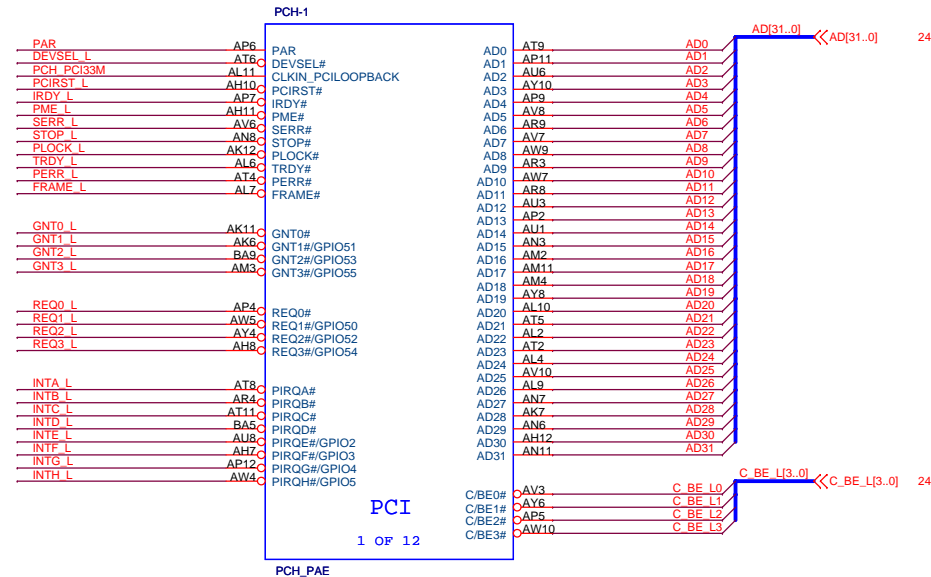




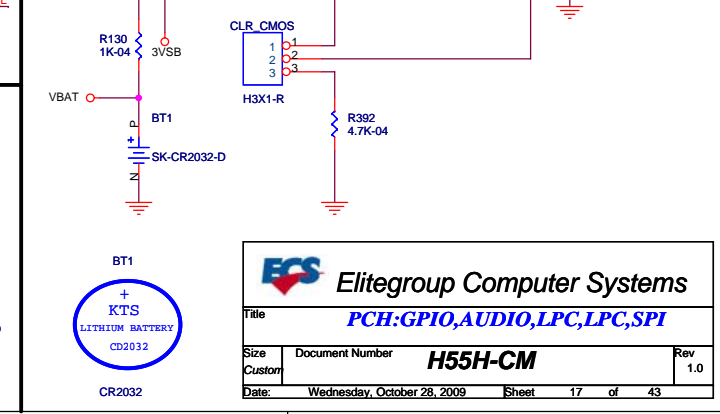
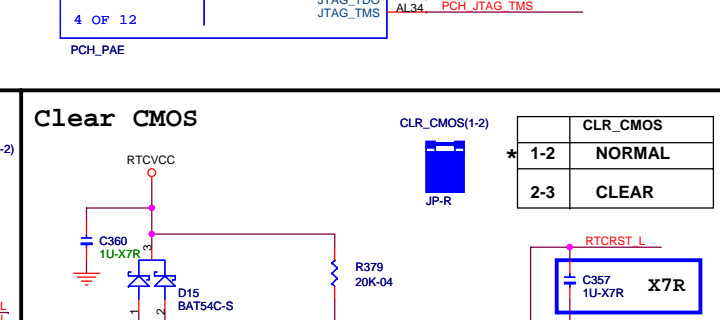
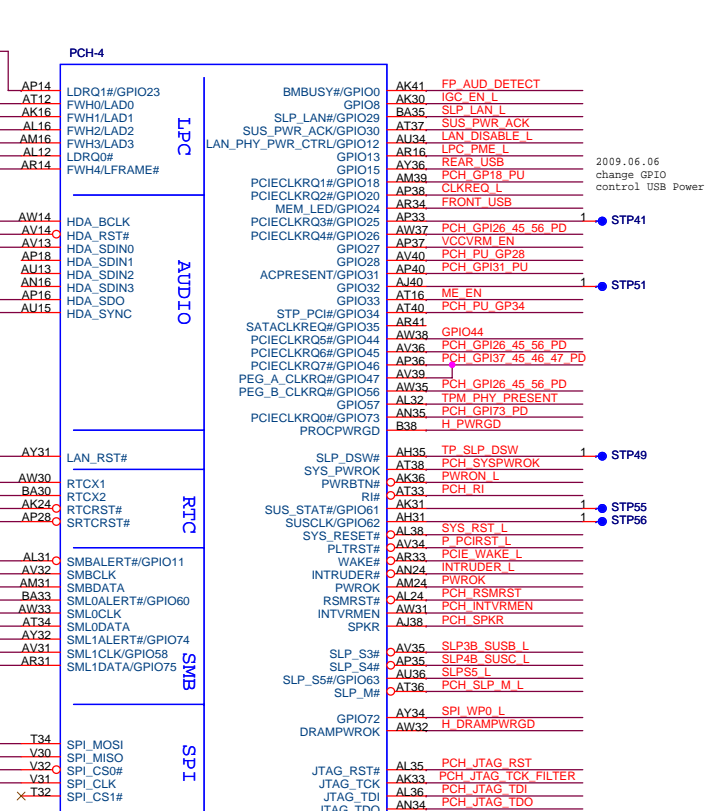
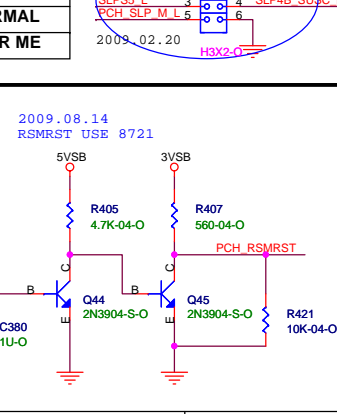
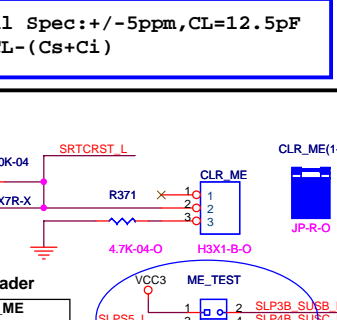
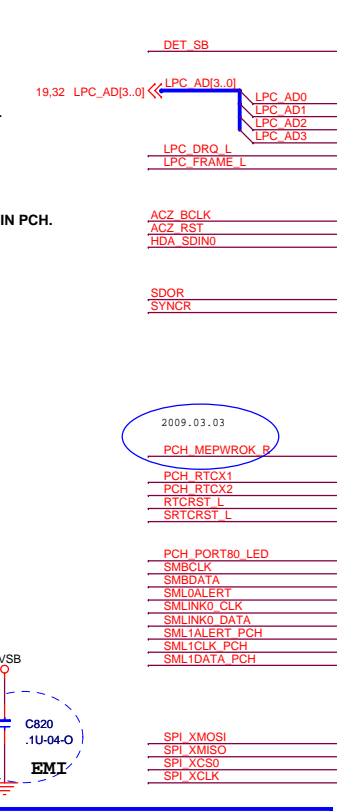
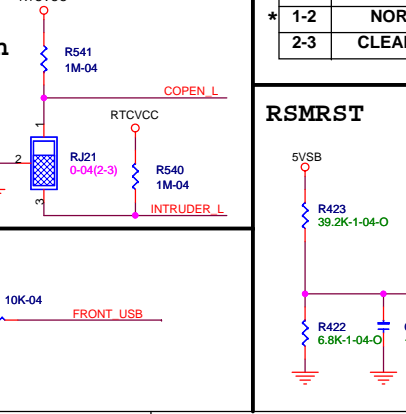
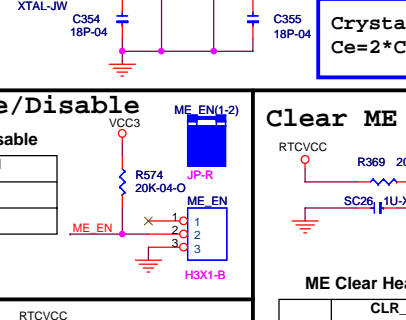
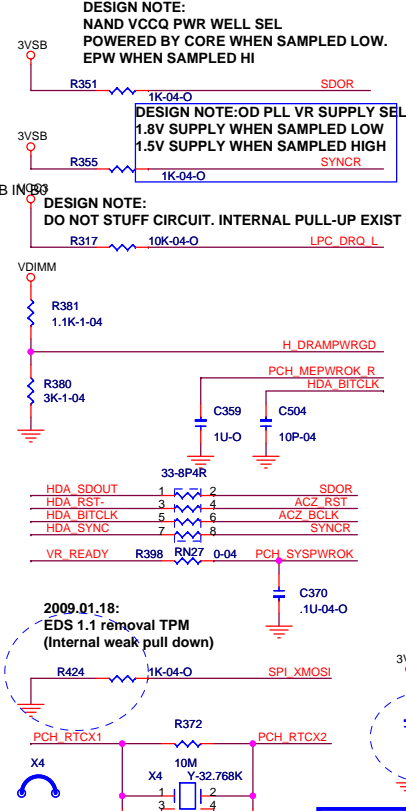
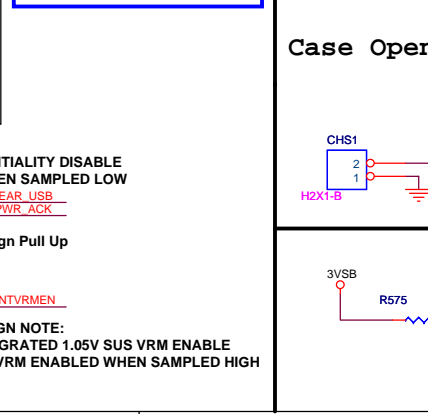
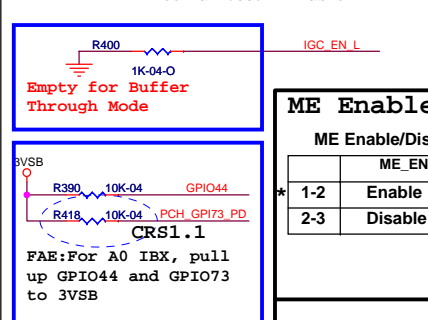
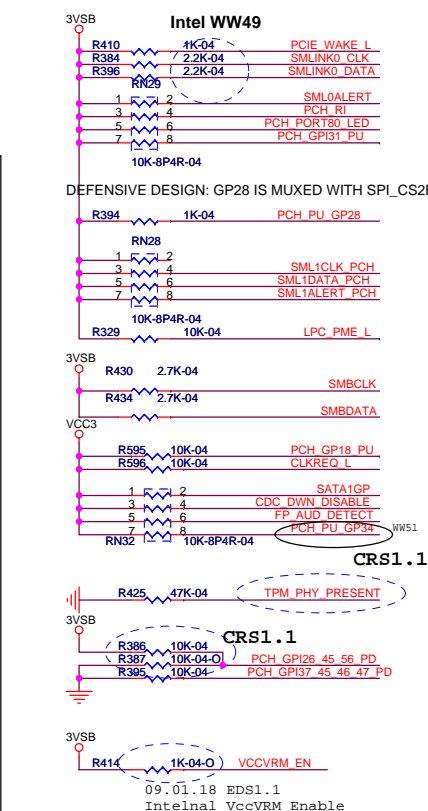
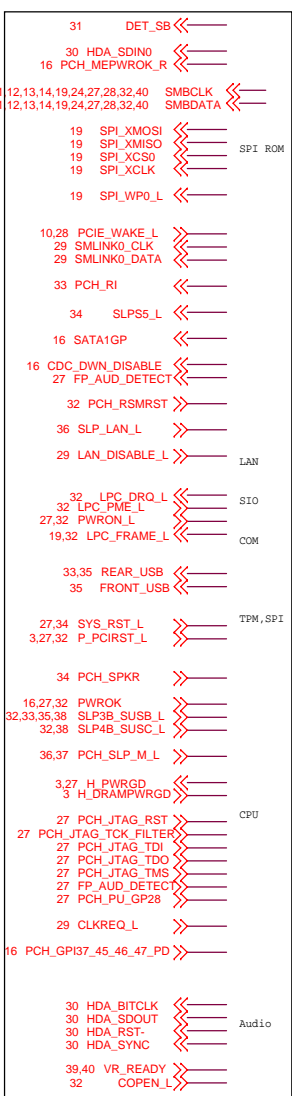
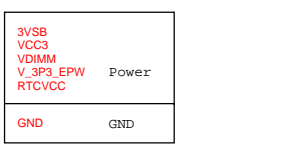
ME_PWROK	
AMT	Ra
Non-AMT	Rb

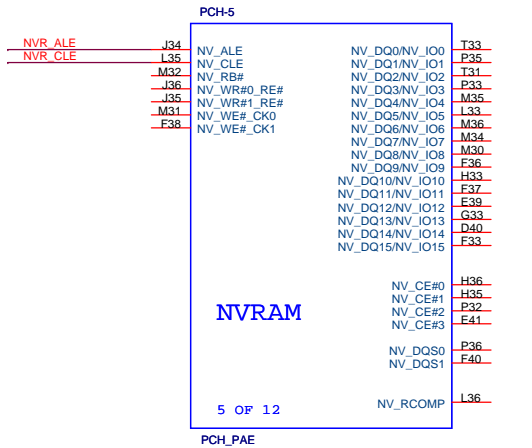
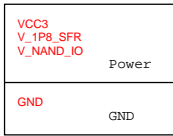


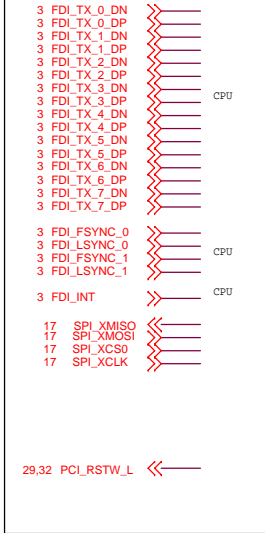
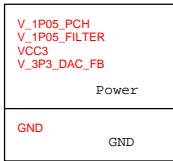
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1





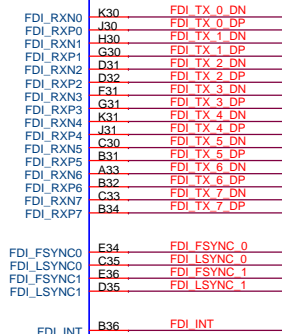






PCH-7

### FDILINK



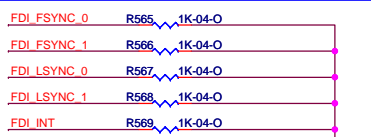
Pipe A

Pipe B

Pipe A

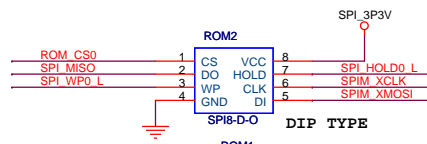
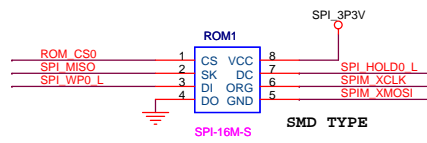
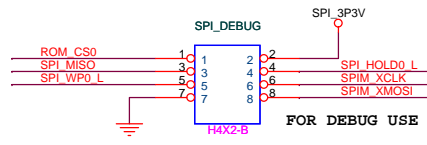
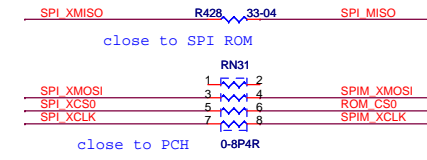
Pipe B

PCH\_PAE



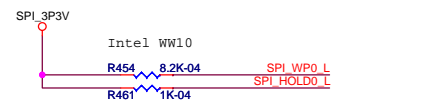
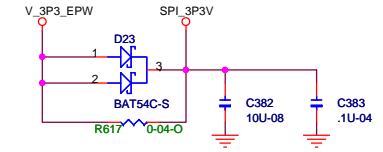
Stuff for Disable FDI

## PCH FDI Link

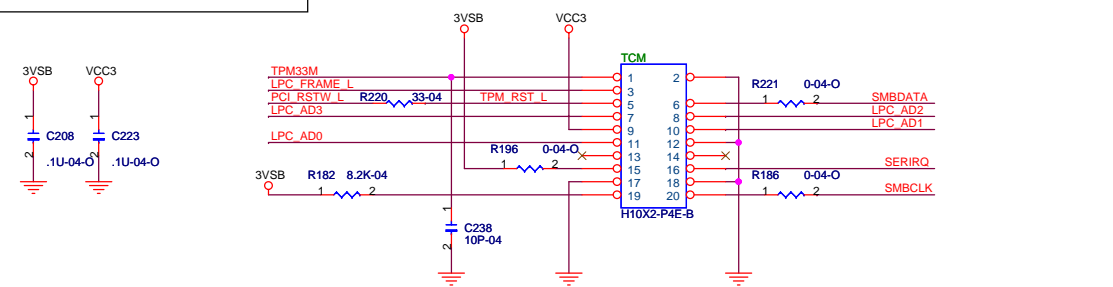
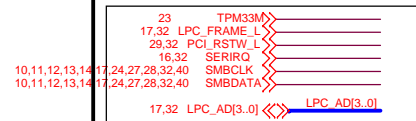


SPI-ROM-4x2

## SPI ROM



	BIOS_WP
Short	Protect
Open	Unprotect



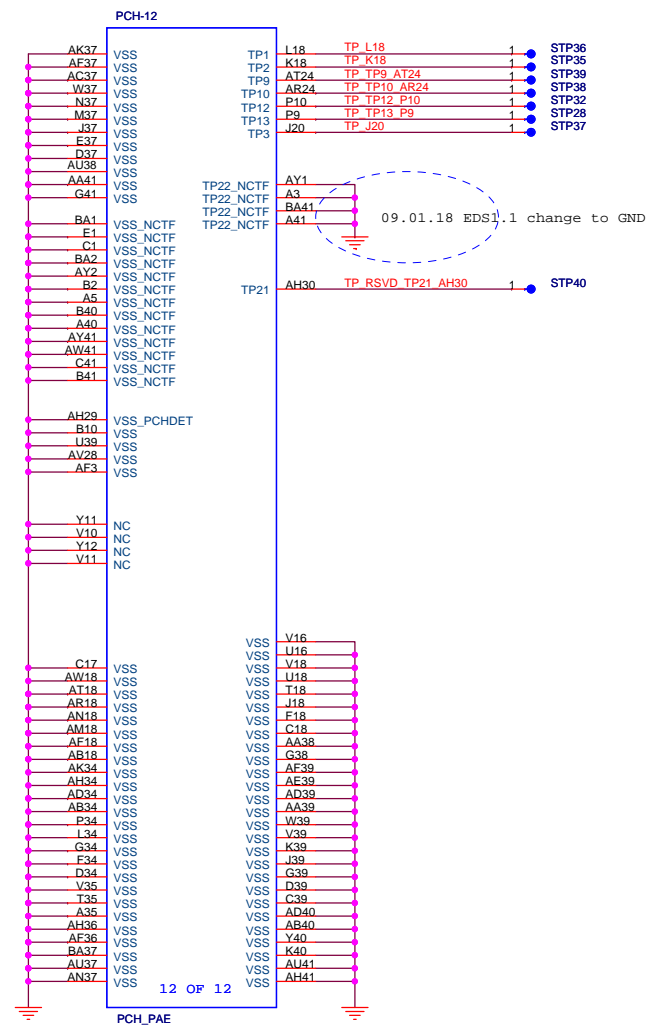
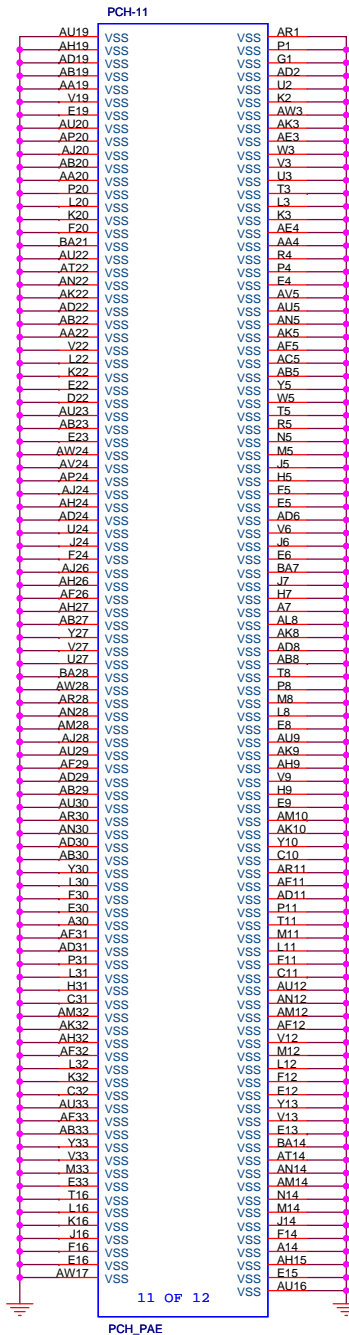
**Elitegroup Computer Systems**

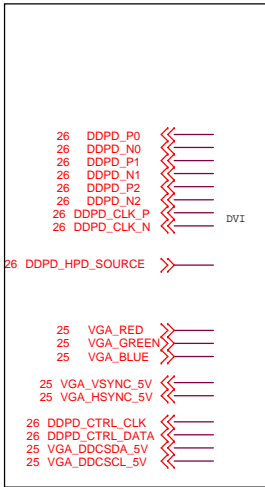
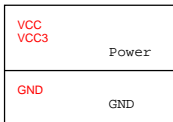
Title **PCH FDLINK & SPI ROM**

Size Document Number **H55H-CM** Rev 1.0

Date: Thursday, October 29, 2009 Sheet 19 of 43

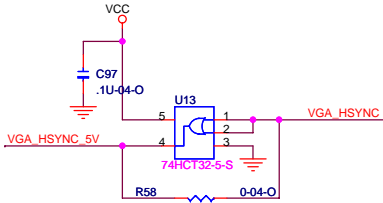
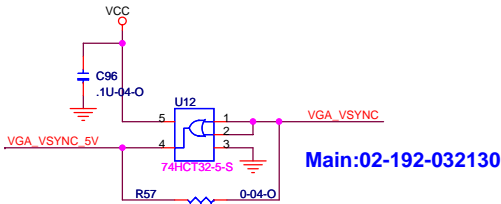
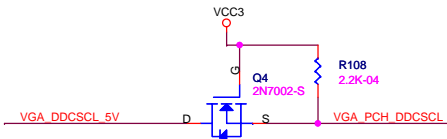
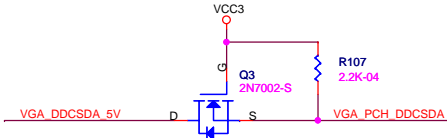
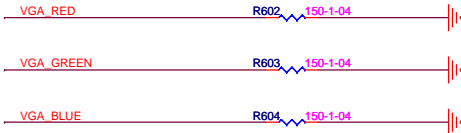
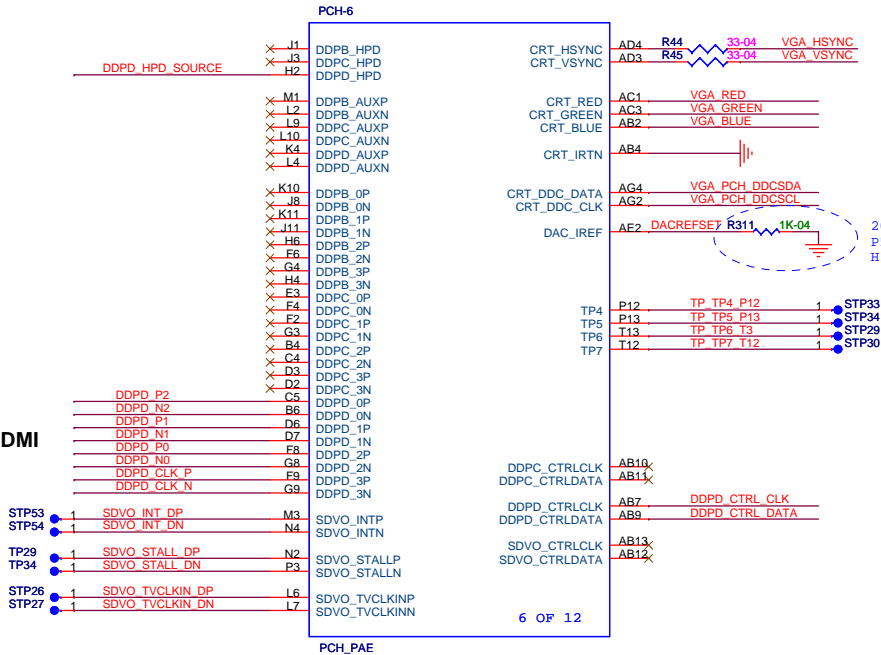




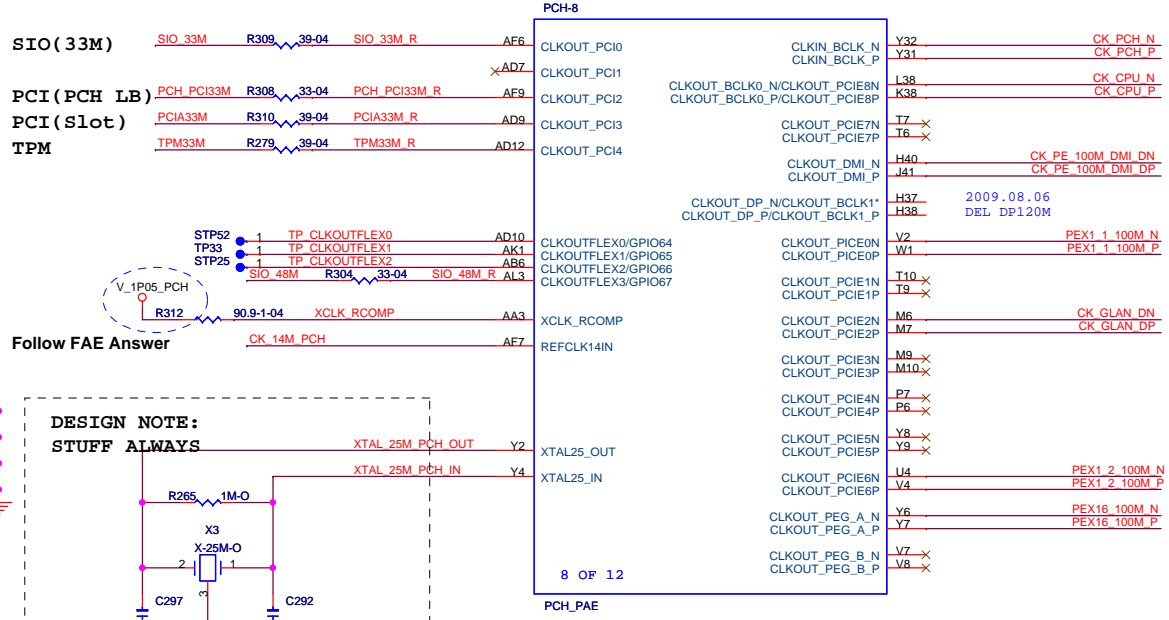
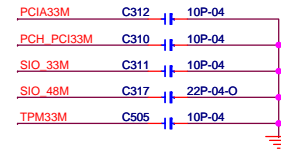
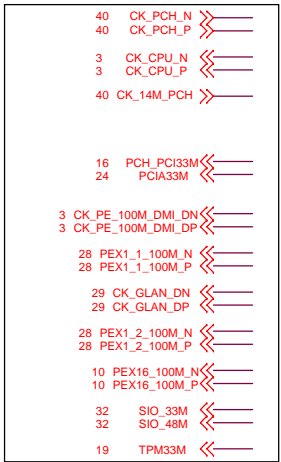
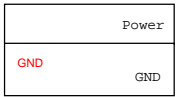


Port B:Capable of SDVO/HDMI/DVI/DP  
Port C:Capable of HDMI/DVI/DP  
Port D:Capable of HDMI/DVI/DP

Port D HDMI



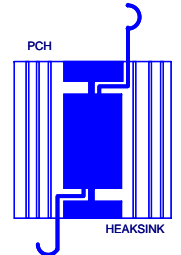
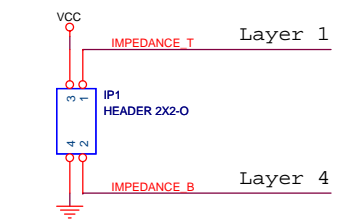
Port	Strap	How to enable the port	How to Disable the Port
Port B	SDVO_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port C	DDPC_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC
Port D	DDPD_CTRLDATA	Pulled the signal high to 3.3V through 2.2K Ohm	NC



DESIGN NOTE:  
STUFF ALWAYS

DESIGN NOTE:  
R128 DAMPING RESISTOR  
DO NOT CHANGE TO 0402

Crystal Spec: +/- 30ppm, CL=20pF  
Ce=2\*CL (Cs+Ci)



Main Part:20-120-013522  
Substitute:20-120-013523

1080 : trace width 4 mil 50 ohm  
Trace Length 3150 mils  
Spacing: 1.clearance to itself 50/4/50(S:W:S)  
2.clearance to other signal 3W

From CLK GEN

CPU(133M)

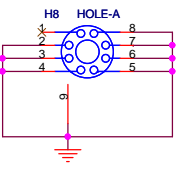
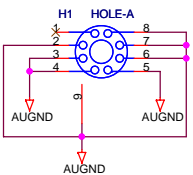
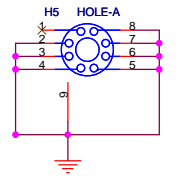
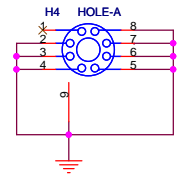
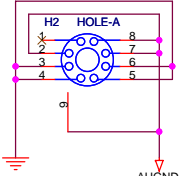
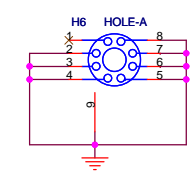
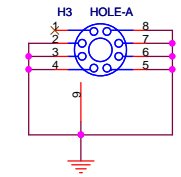
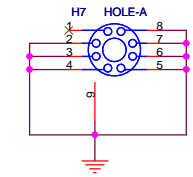
CPU(DMI)

PCIE (X1)

Giga LAN

PCIE(1X2)

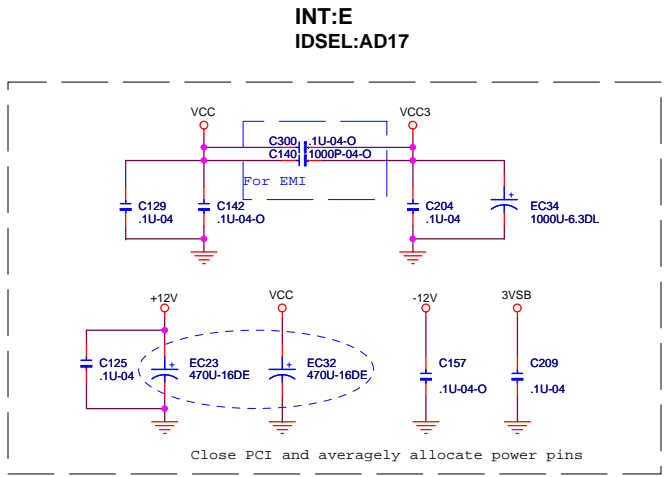
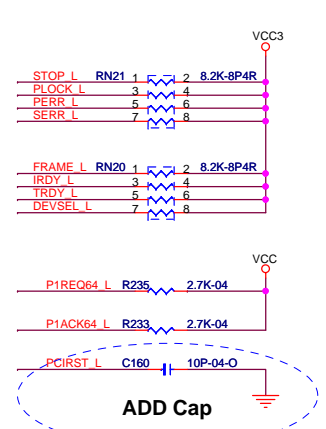
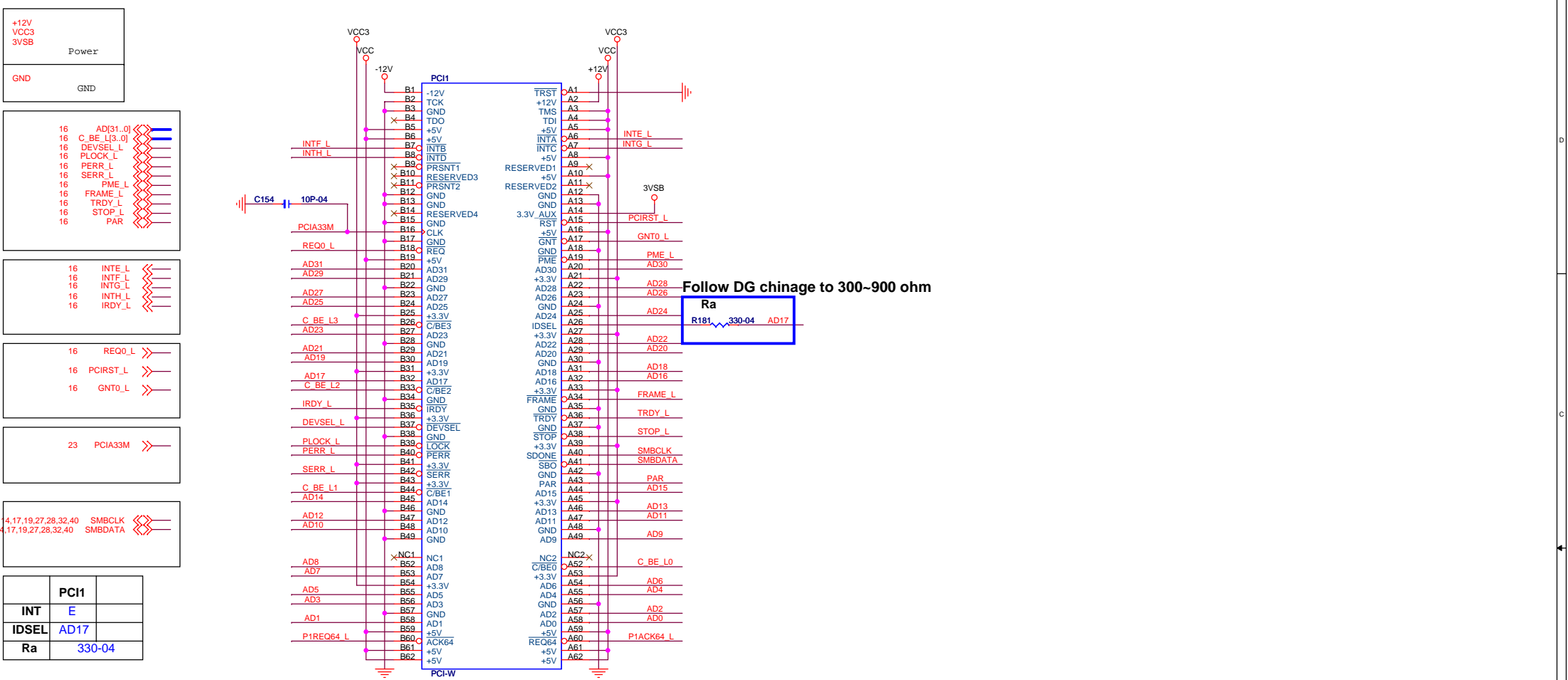
PCIE(16X)



Title: **PCH CLOCKS,STRAPS**

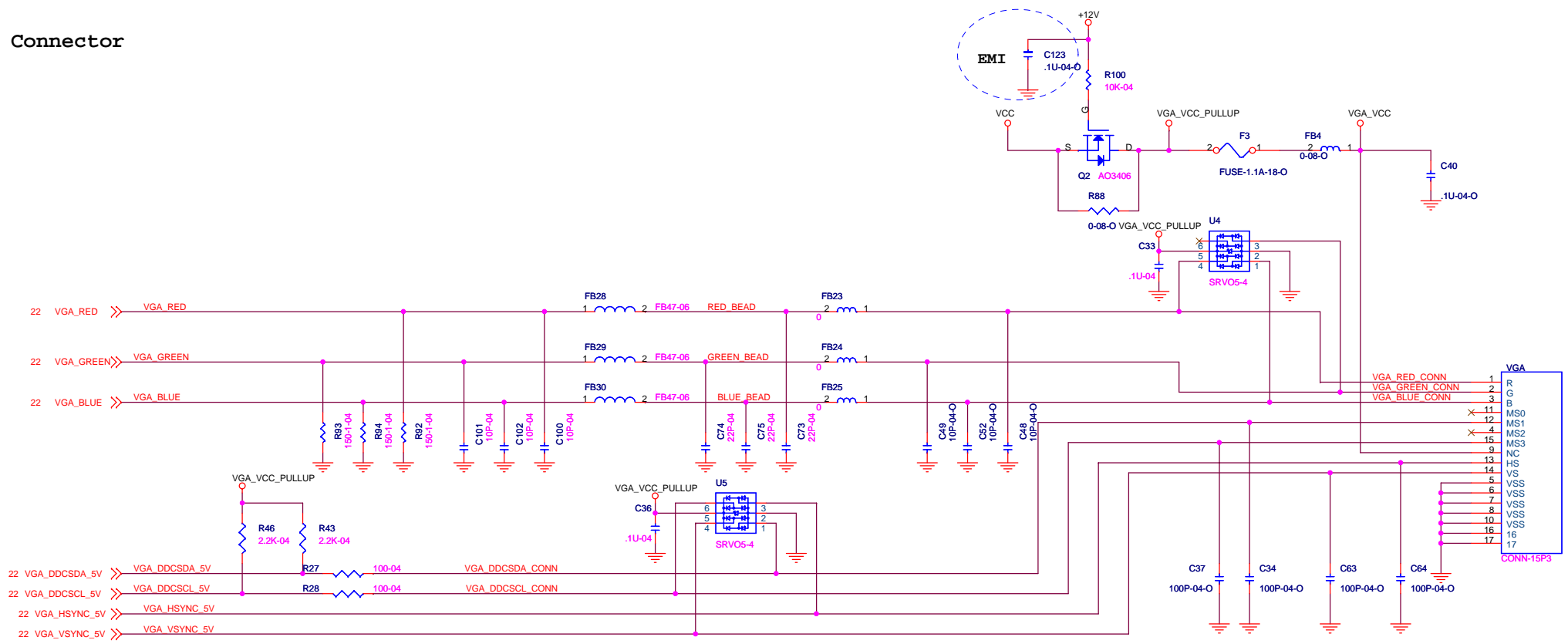
Size: Custom Document Number: **H55H-CM** Rev: 1.0

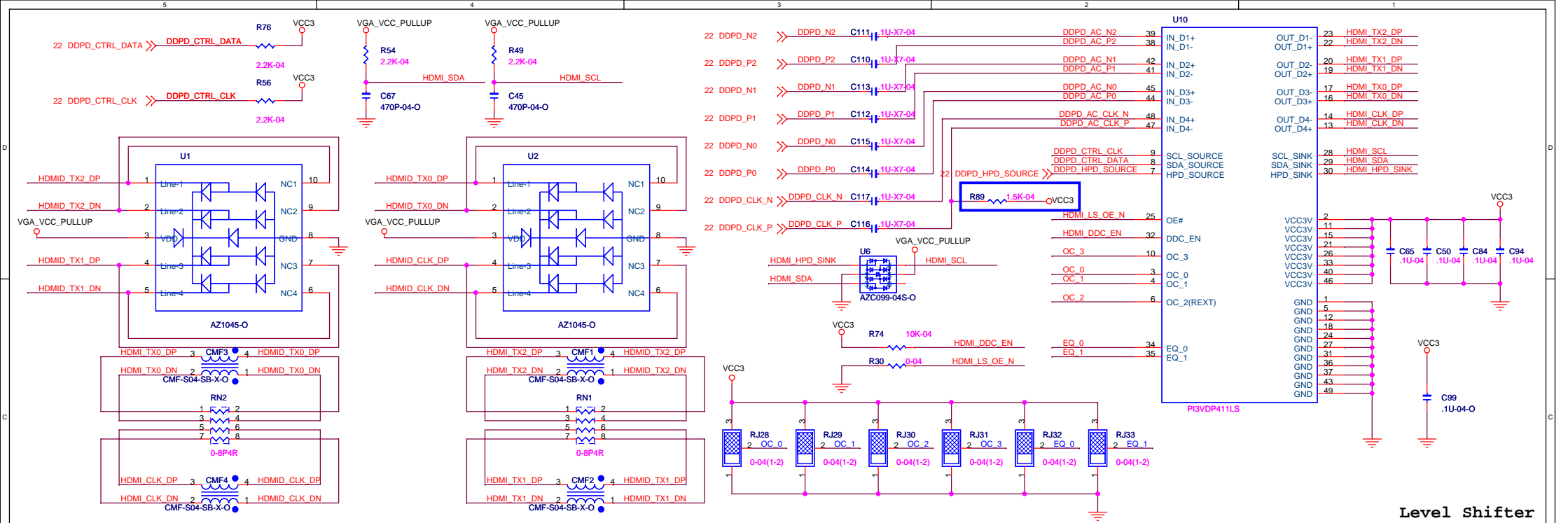
Date: Thursday, September 17, 2009 Sheet: 23 of 43



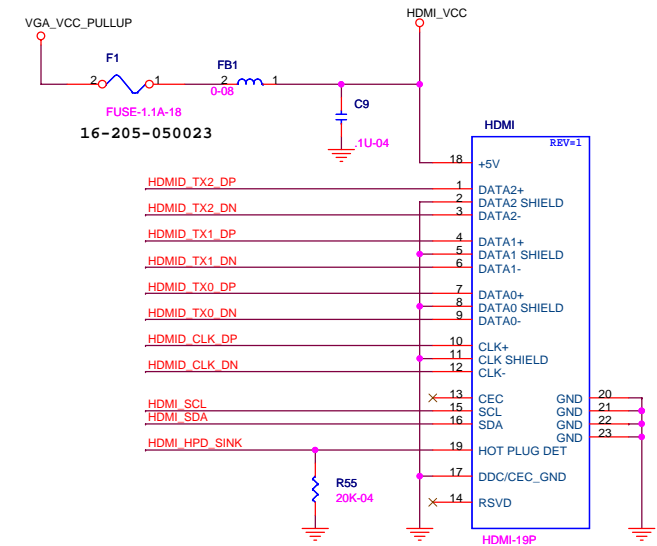


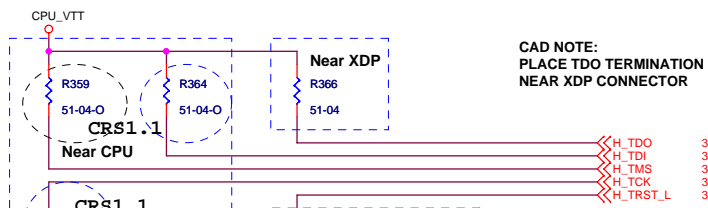
VGA Connector



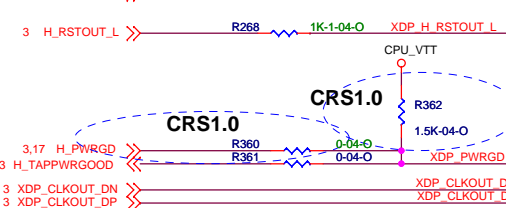
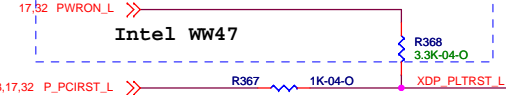
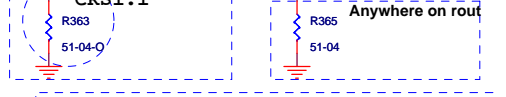


## HDMI Connector

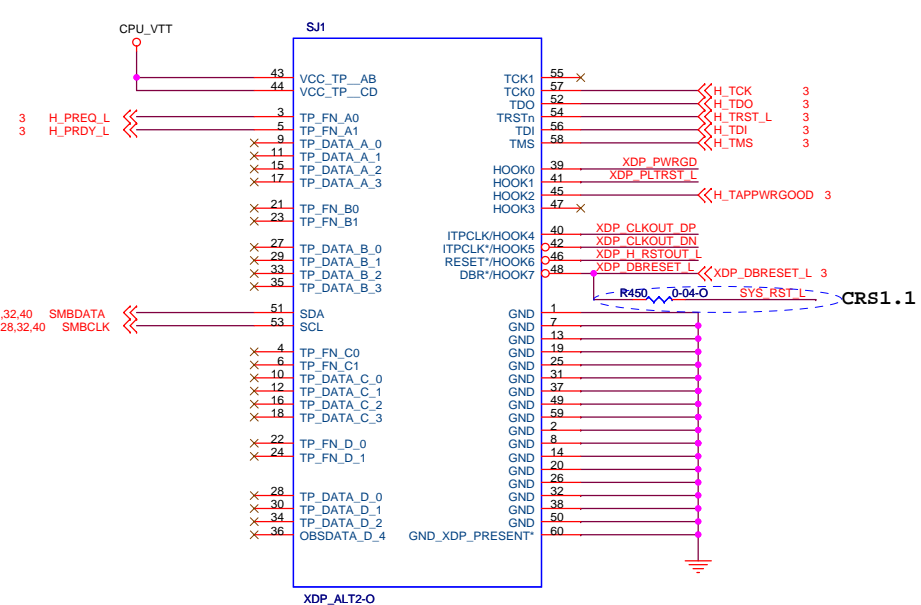
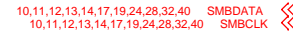
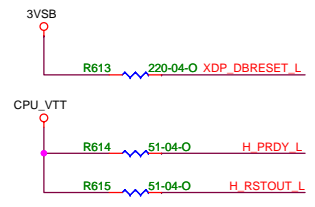




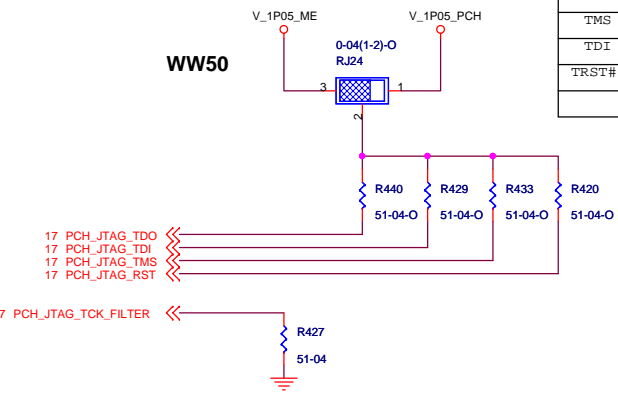
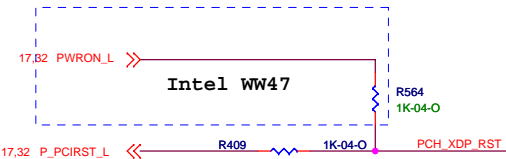
CAD NOTE:  
PLACE TDO TERMINATION  
NEAR XDP CONNECTOR



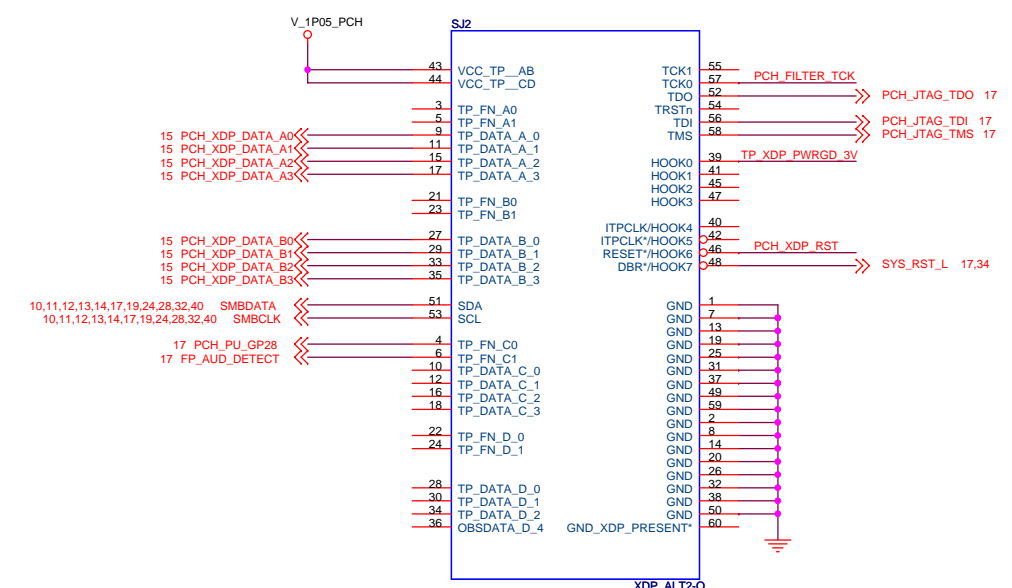
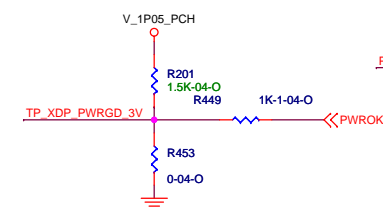
CLK Source:Default use PCH



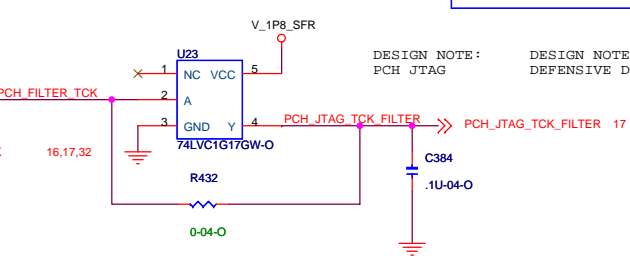
DESIGN NOTE:  
DEFAULT EMPTY SITE ON PAGE 94: XDP\_PWRGD RES (R108PR) TO VTT\_OUT\_RIGHT  
DEFAULT EMPTY SITE ON PAGE 123: XDP\_PWRGD RES (R3S3EV) TO V\_FSB\_VTT  
DEFAULT STUFF SITE: (R662EV) TO TP\_XDP\_PWRGD

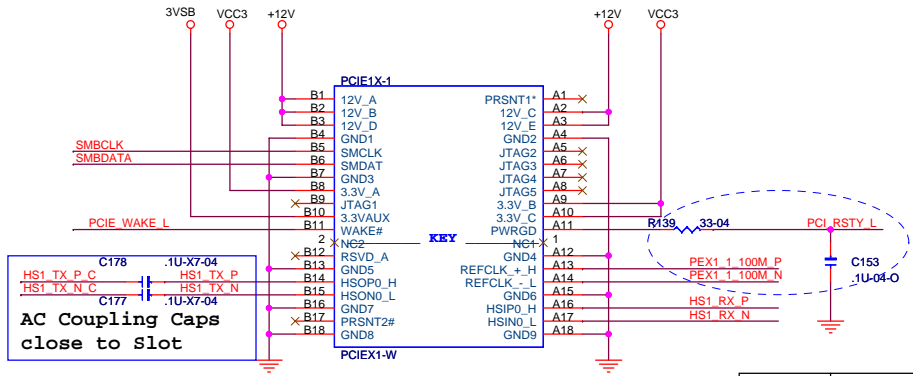
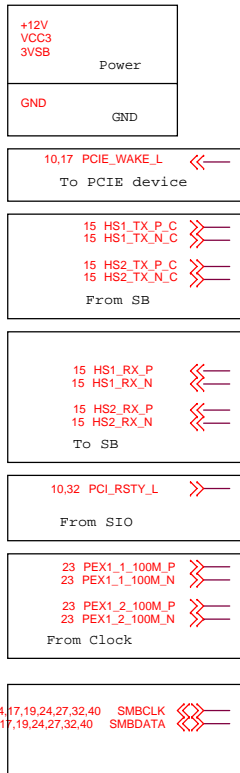
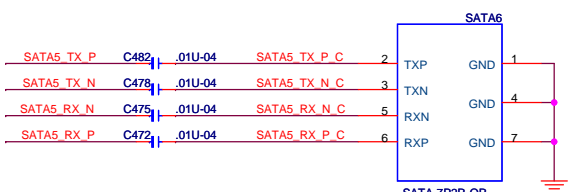
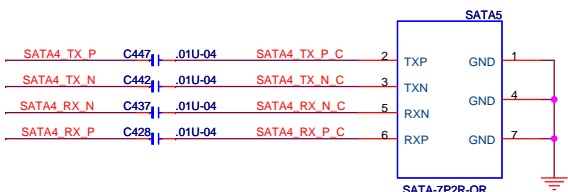
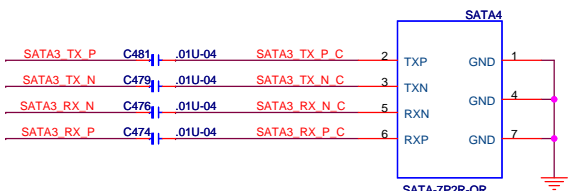
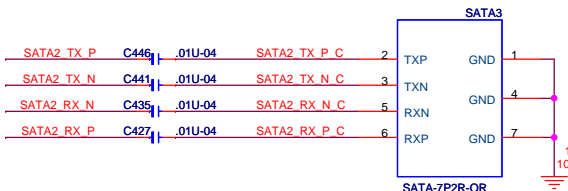
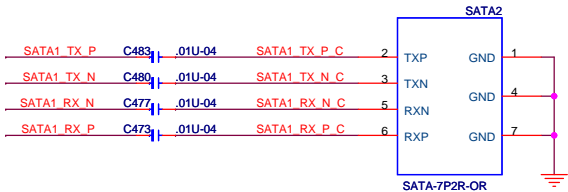
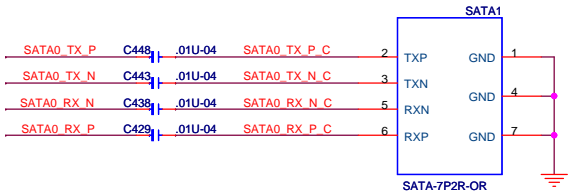
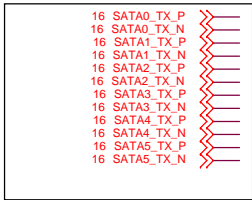


PCH PIN	RefDes	ES1	ES2	Production Systems
TDO	R440	No Stuff	100 Ohms	51 Ohms
TMS	R433	100 Ohms	100 Ohms	51 Ohms
TDI	R429	100 Ohms	100 Ohms	51 Ohms
TRST#	R420	10K Ohms	10K Ohms	51 Ohms
	RJ24	0 (2-3)	0 (2-3)	0 (1-2)

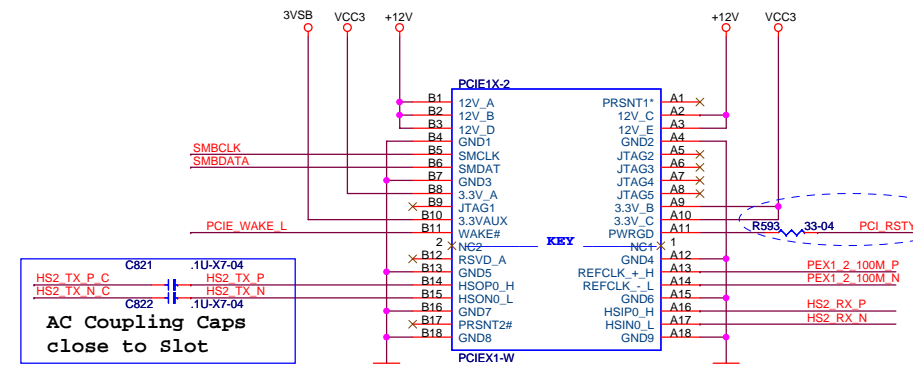
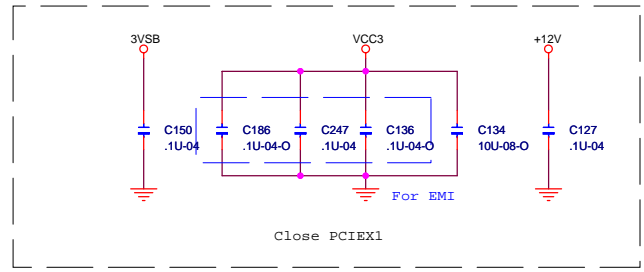


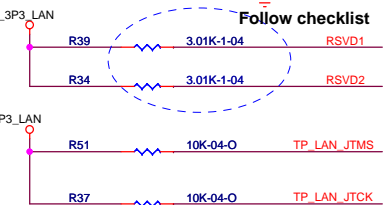
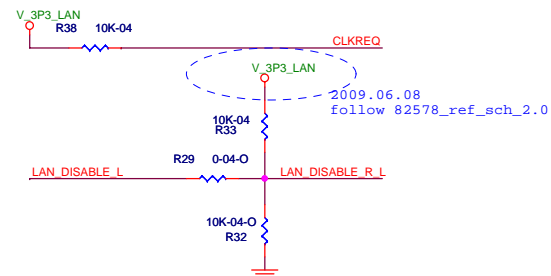
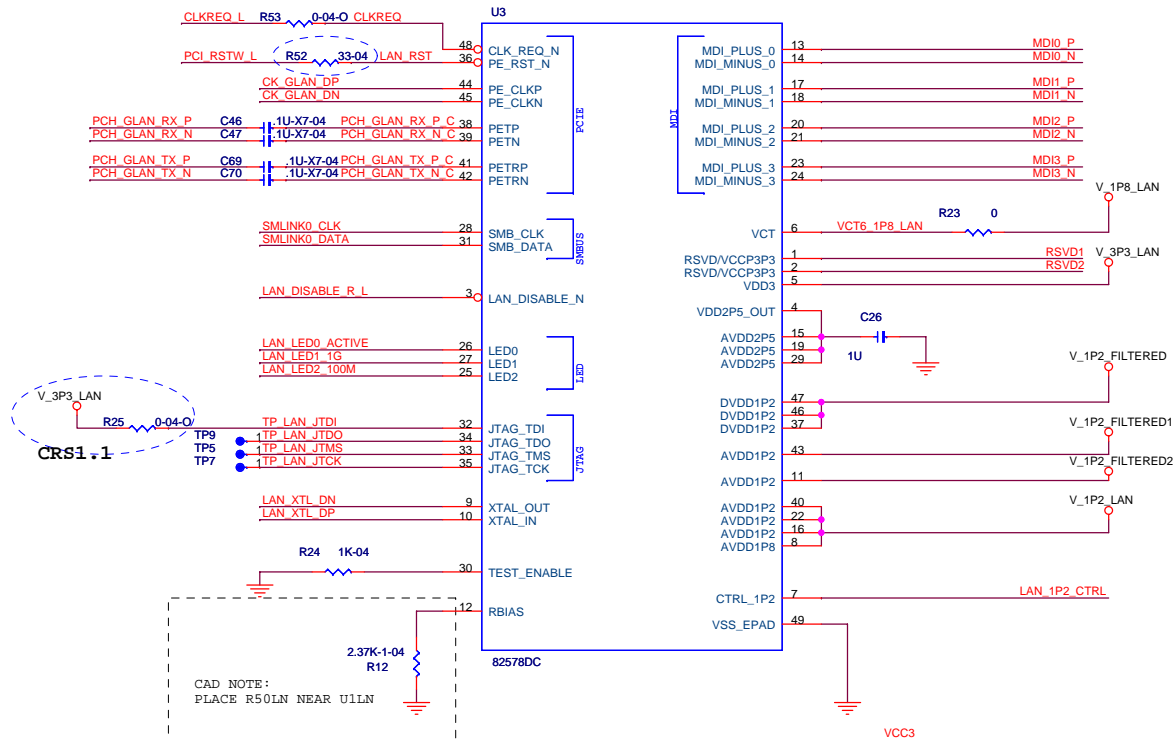
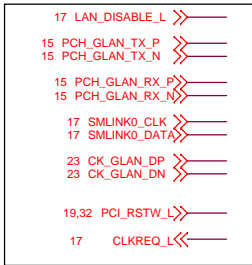
DESIGN NOTE:  
PCH JTAG  
DEFENSIVE DESIGN



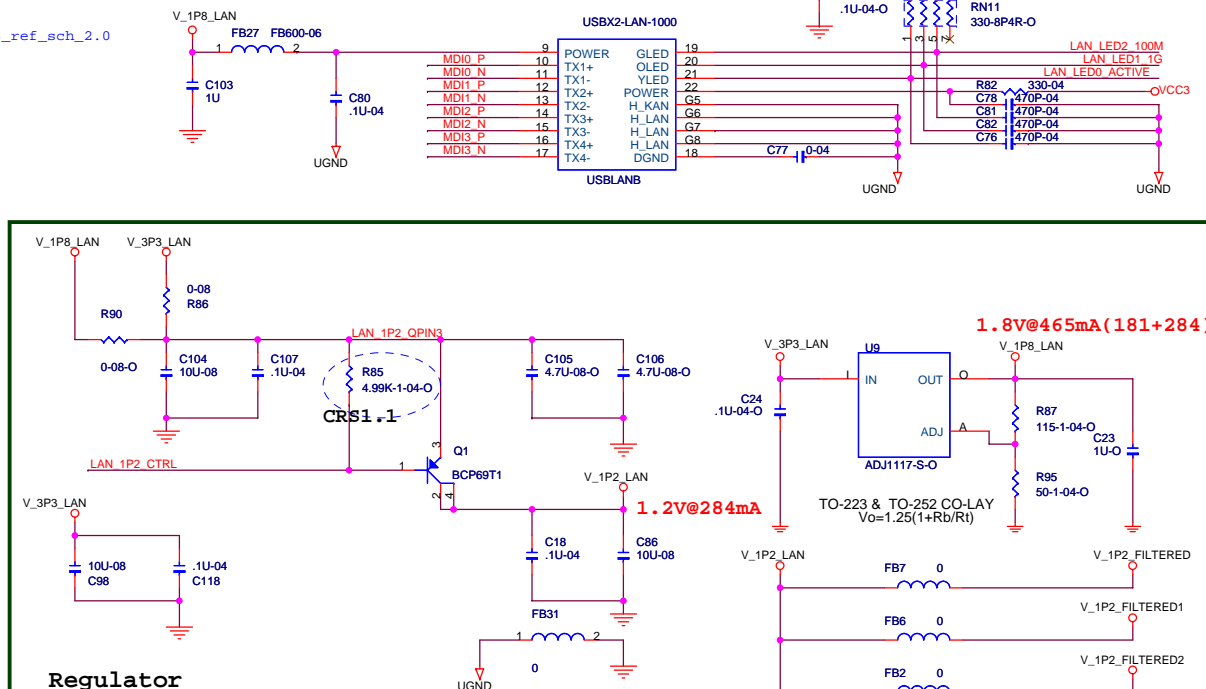


	PC_RST
INTEL	SIO:PCI REST
AMD	NB:PCI REST
NV?	

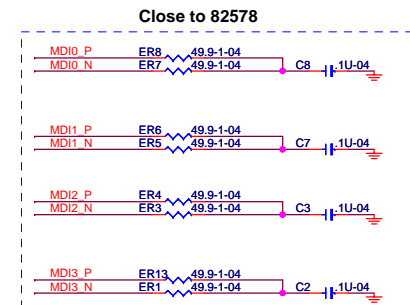
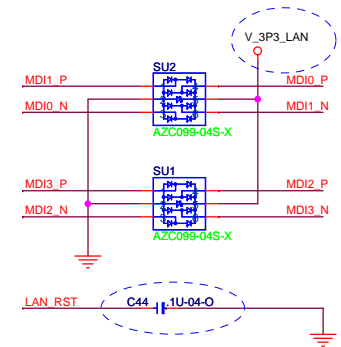




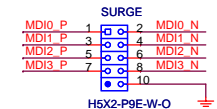
LAN\_XTL\_DP



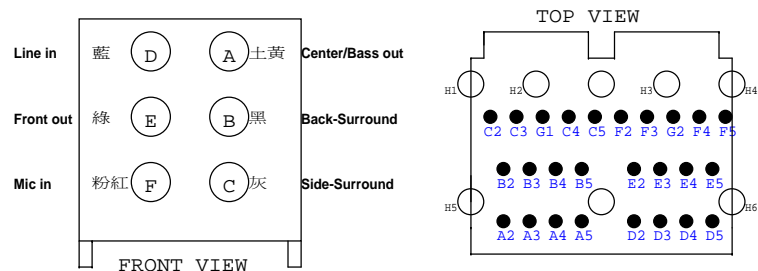
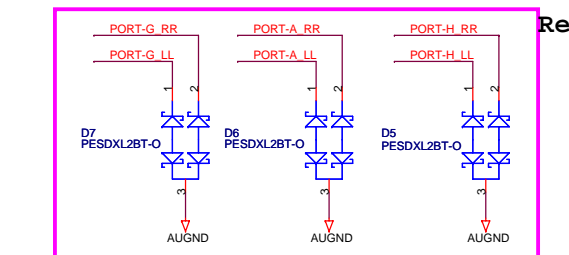
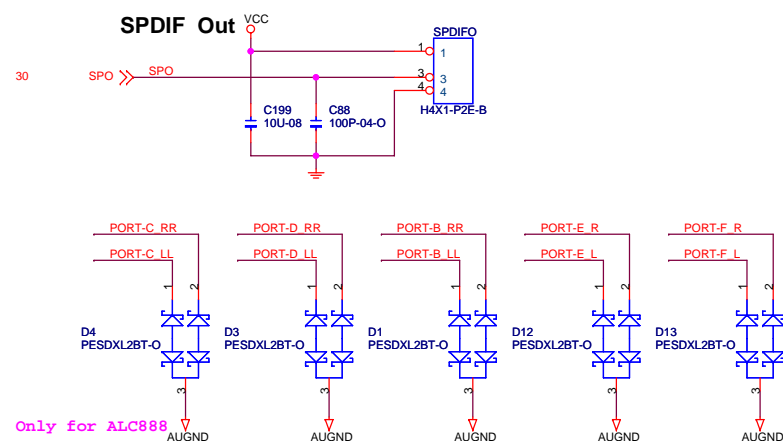
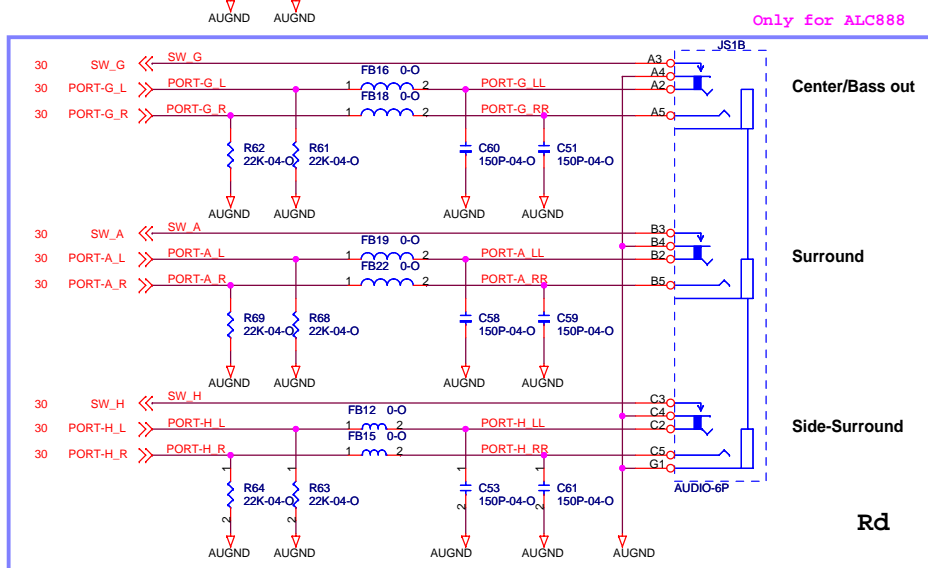
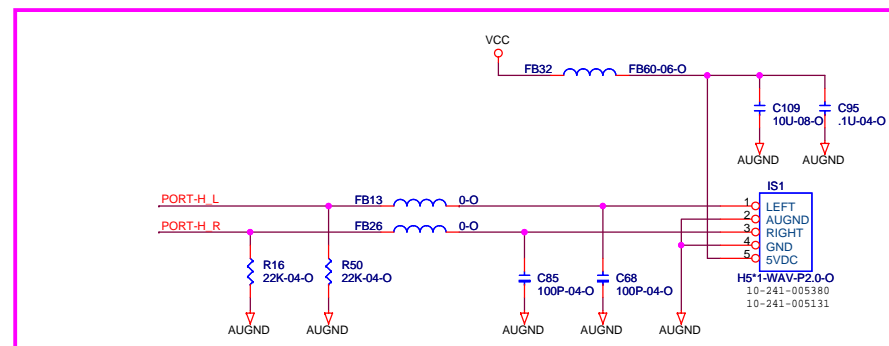
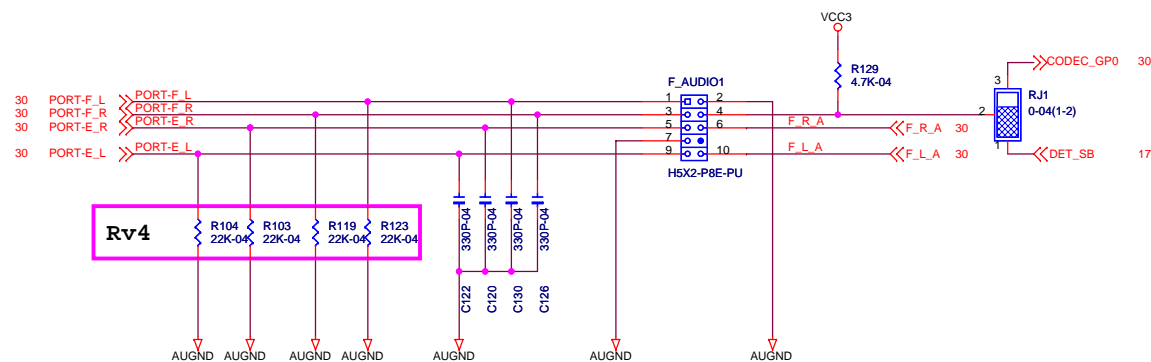
Remark: Y/G/O-->Color, B-->Blinking



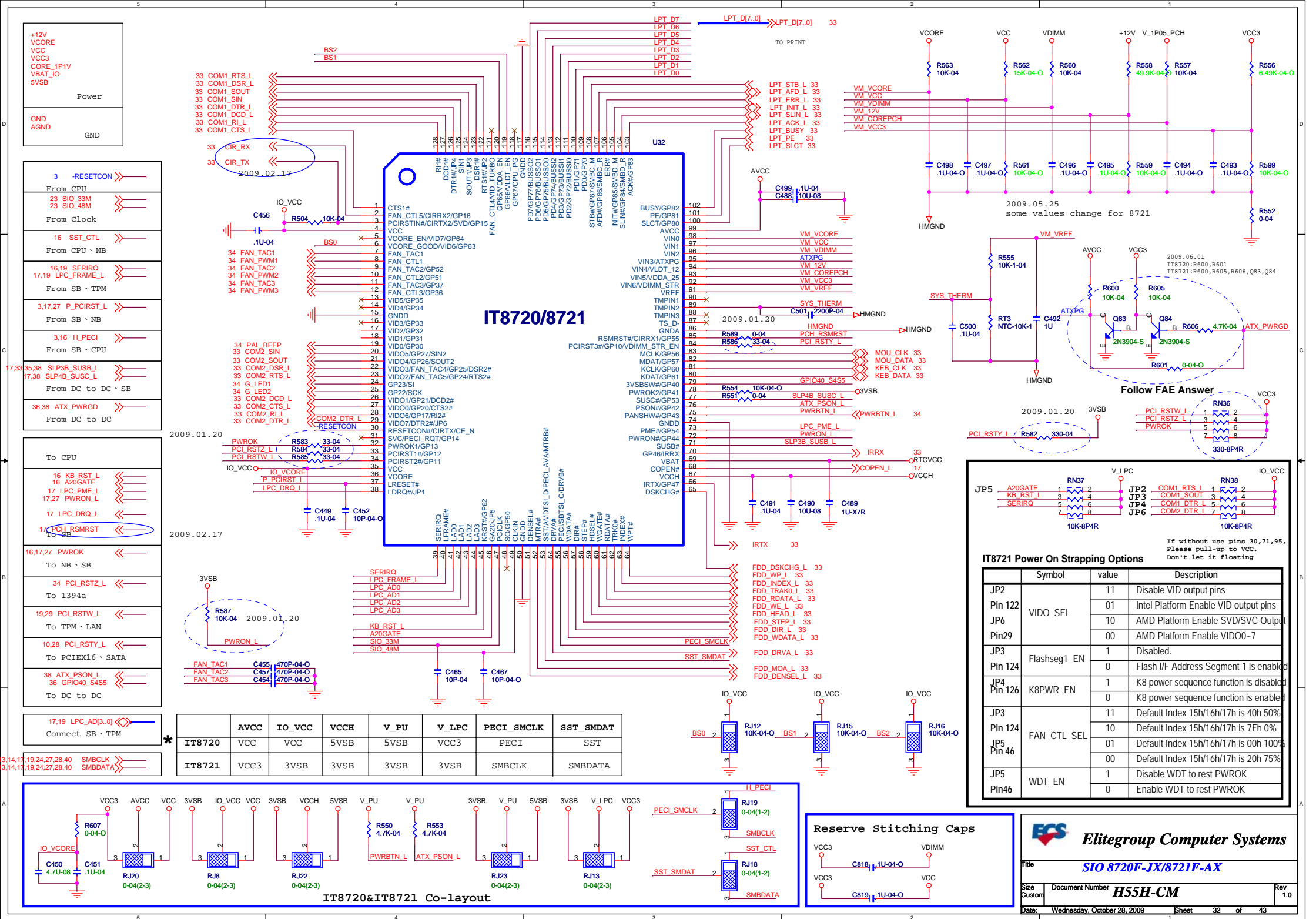
### Surge for TongFang







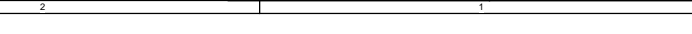
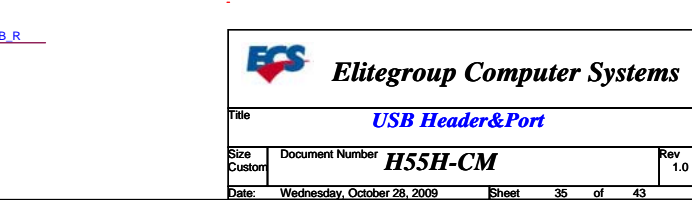
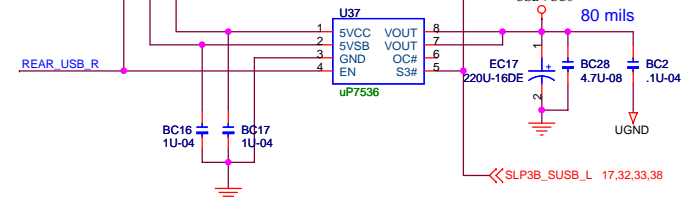
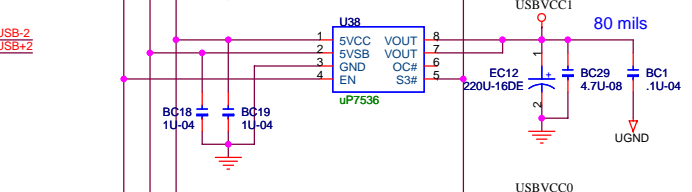
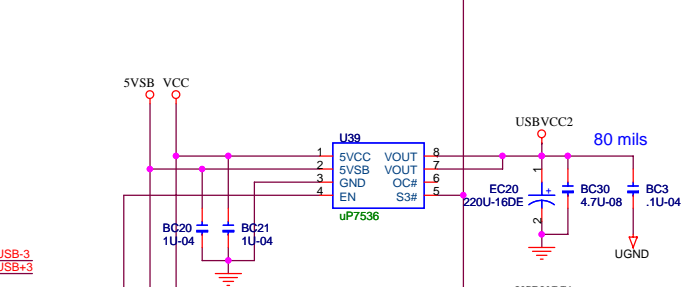
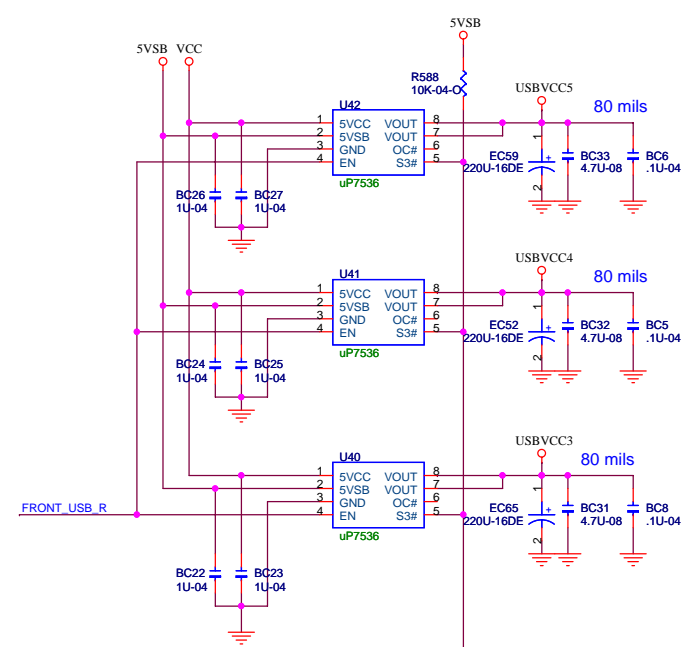
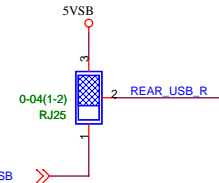
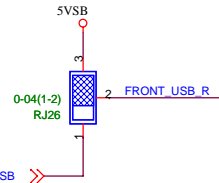
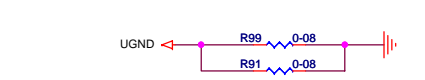
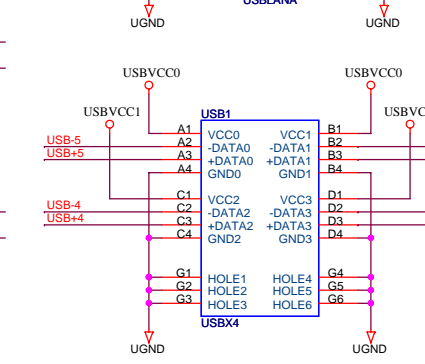
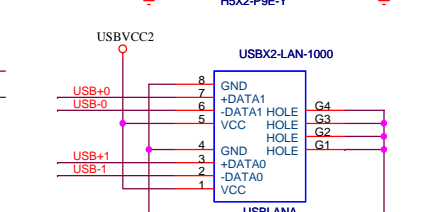
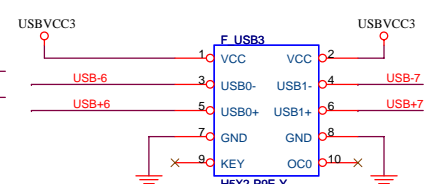
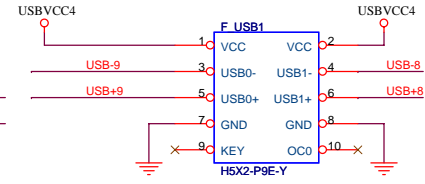
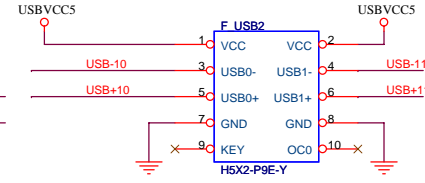
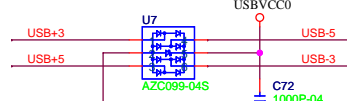
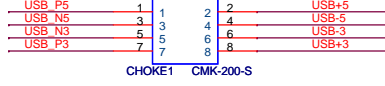
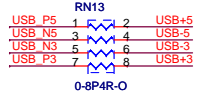
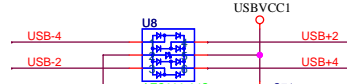
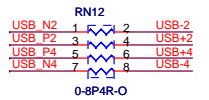
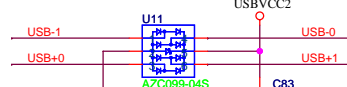
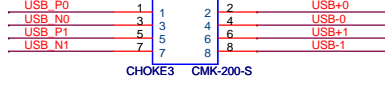
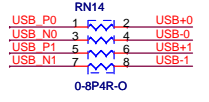
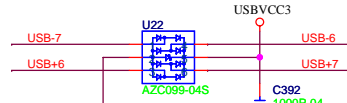
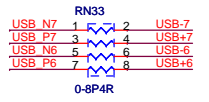
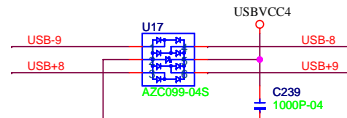
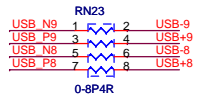
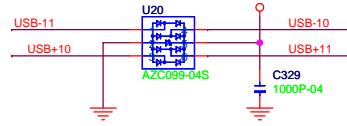
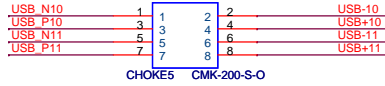
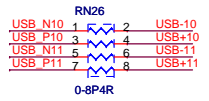
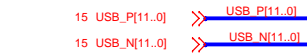












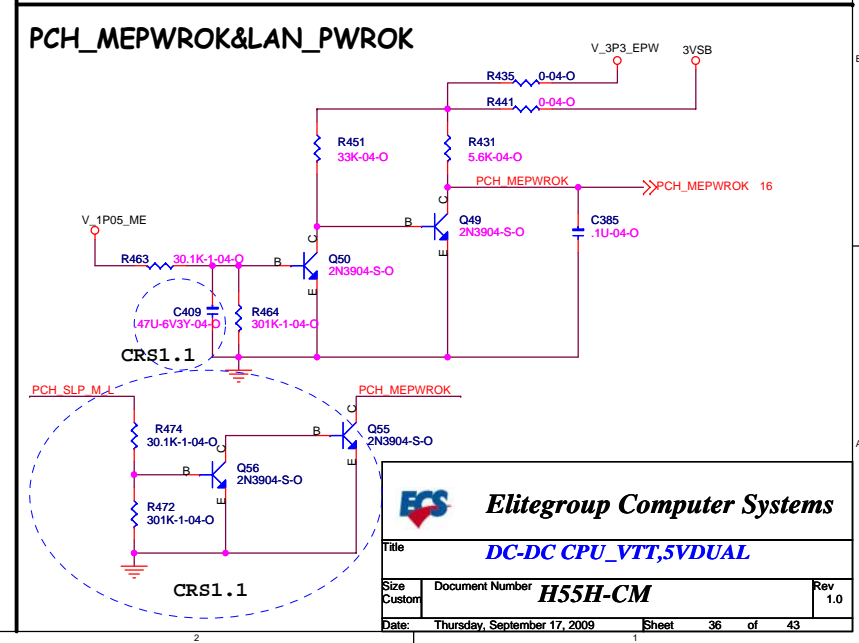
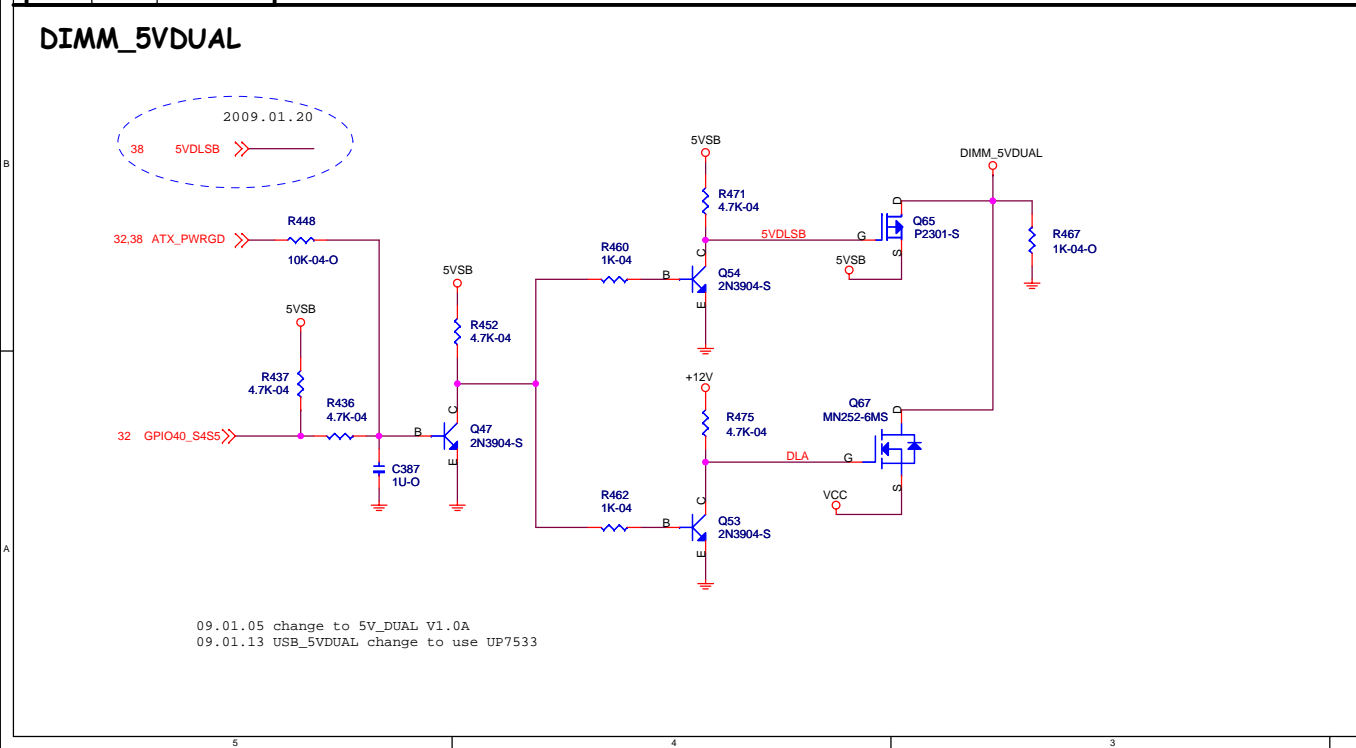
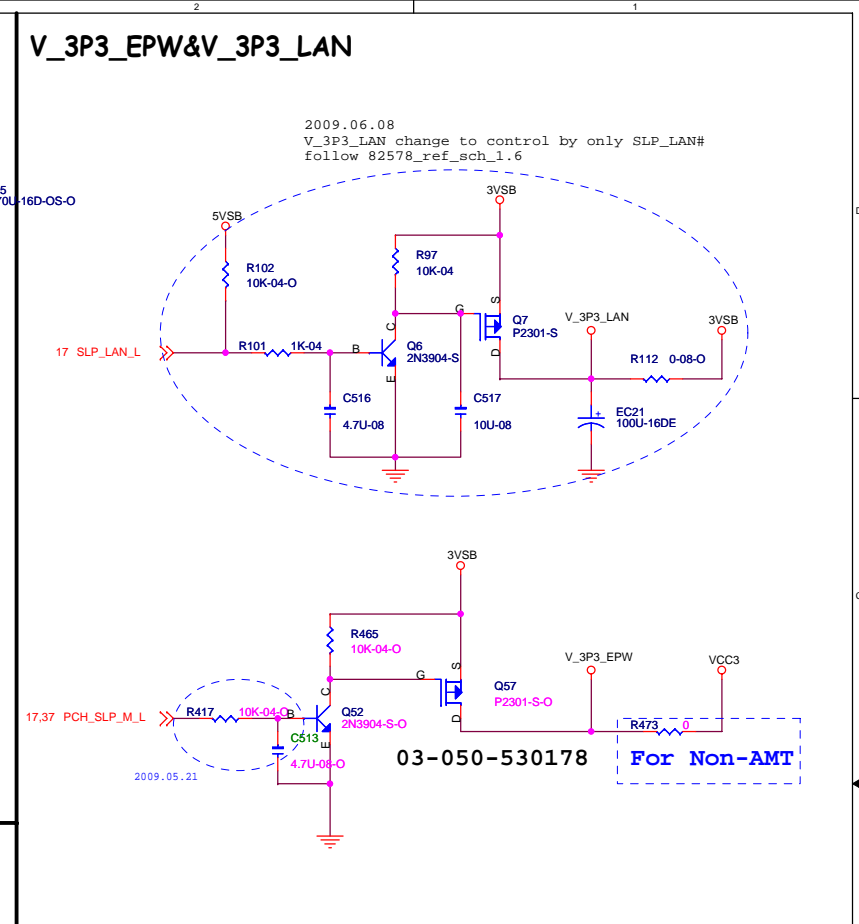
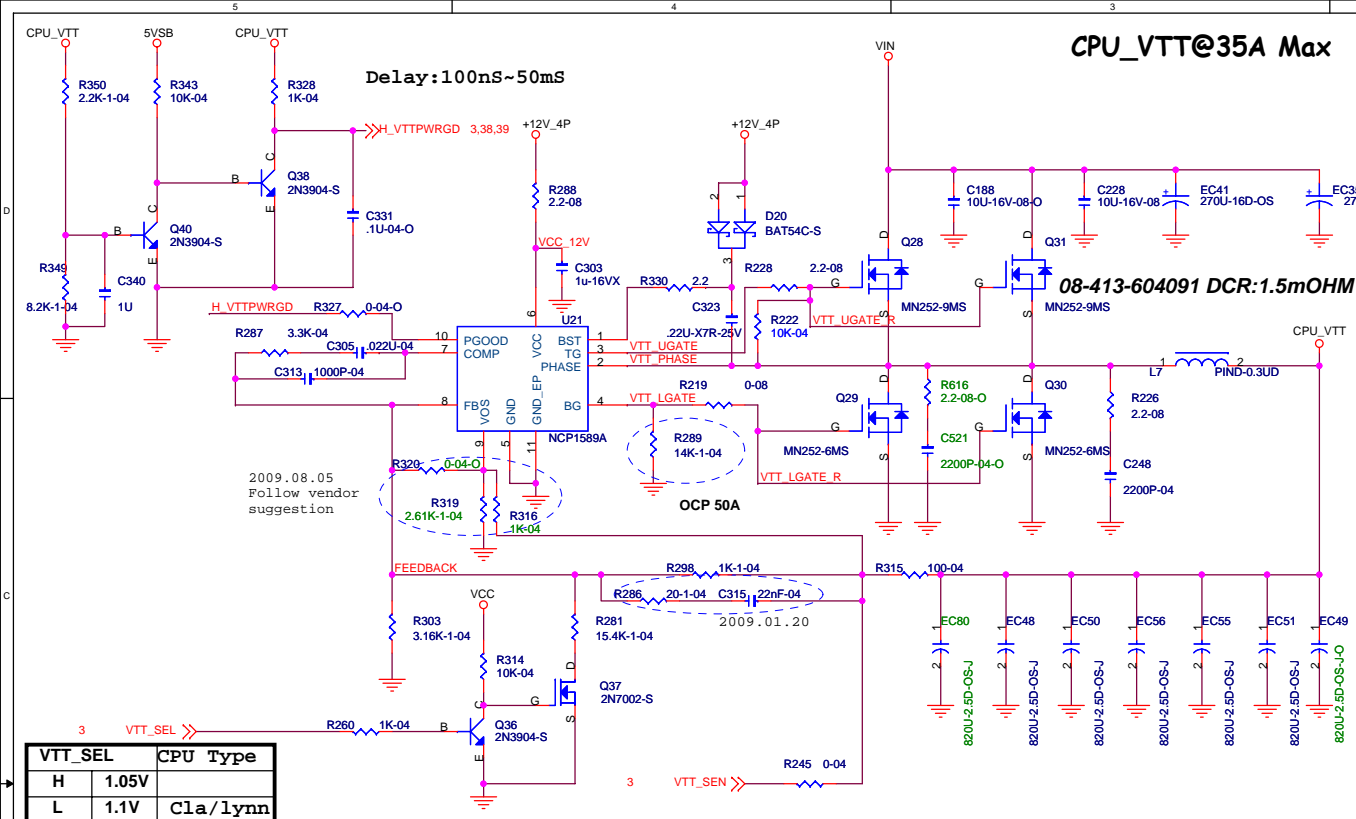
**Elitegroup Computer Systems**

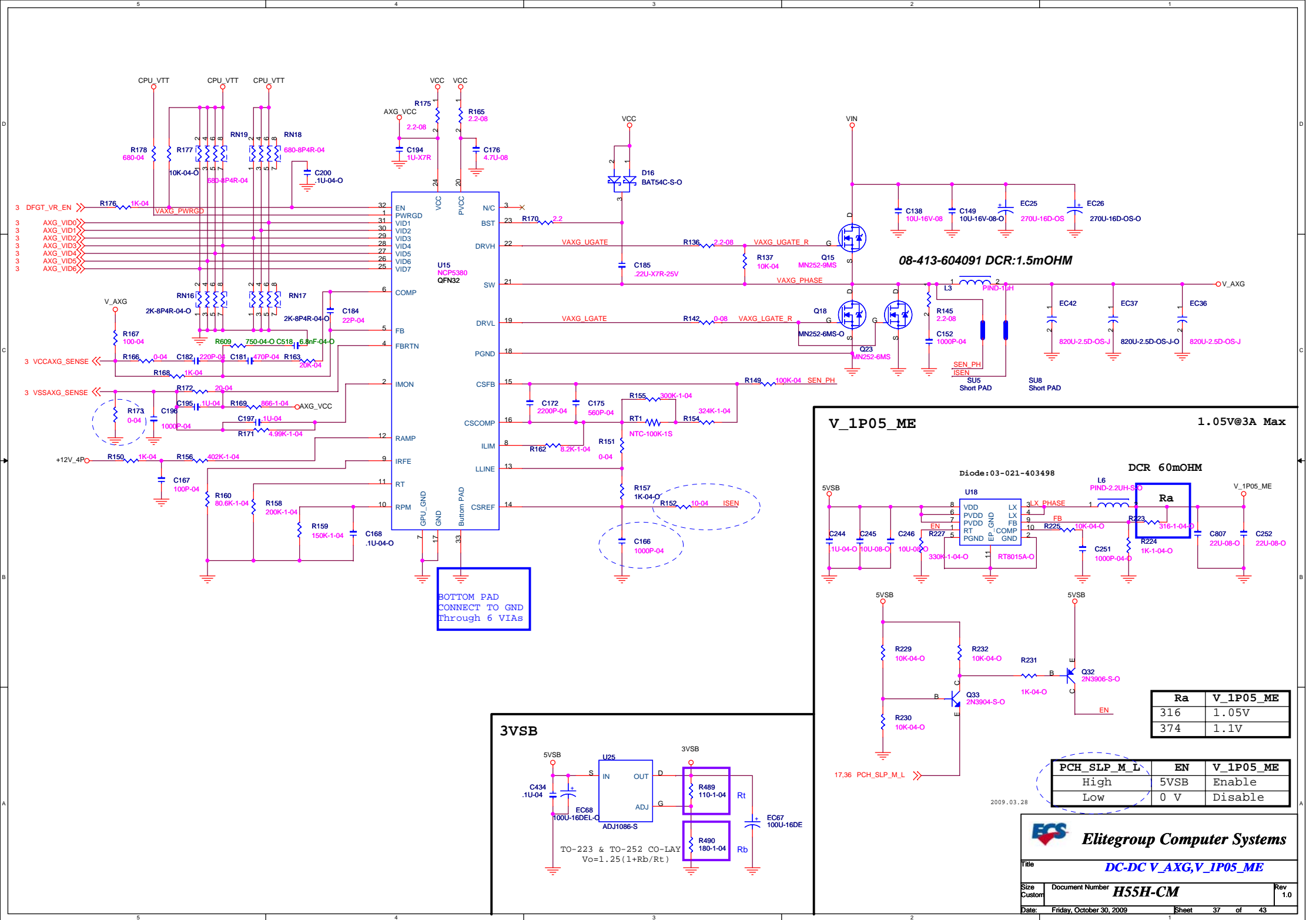
**USB Header&Port**

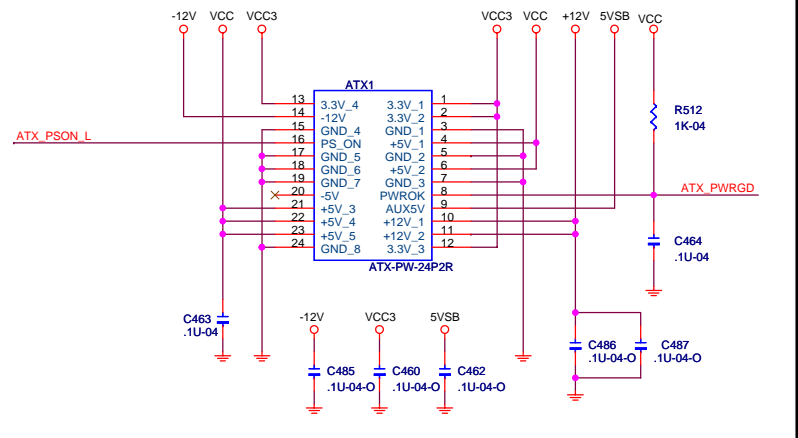
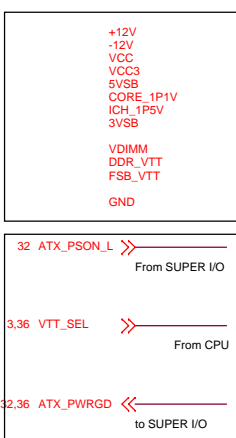
Title: **USB Header&Port**

Size: Document Number **H55H-CM** Rev 1.0

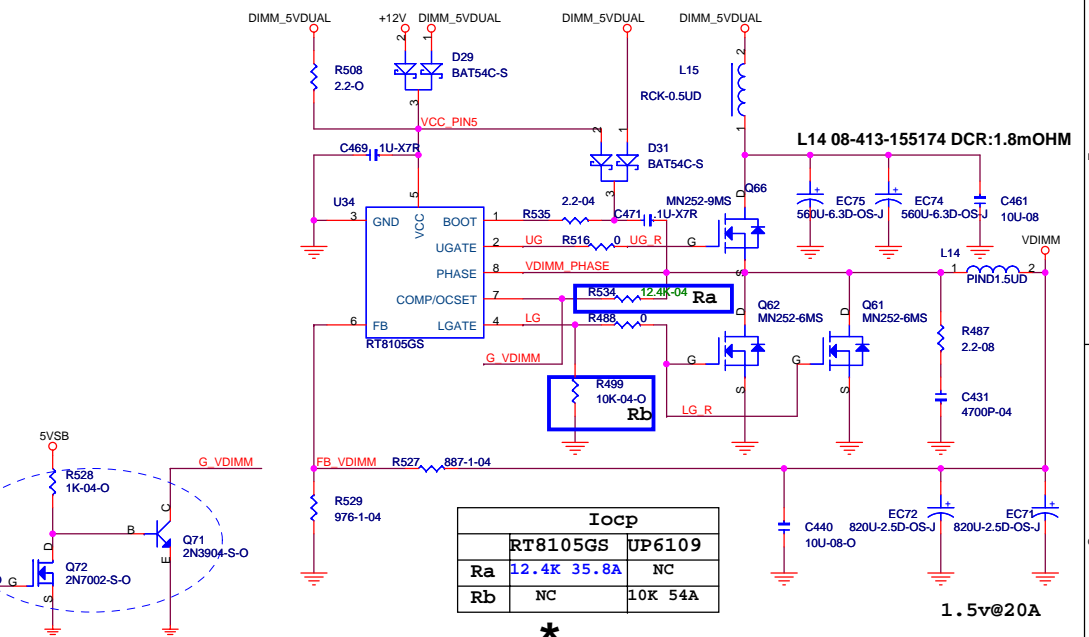
Date: Wednesday, October 28, 2009 Sheet 35 of 43



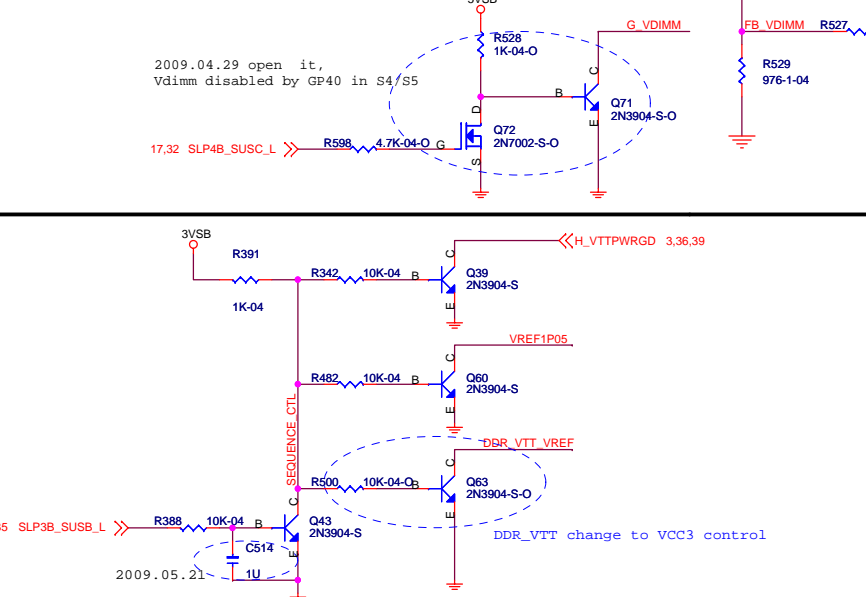
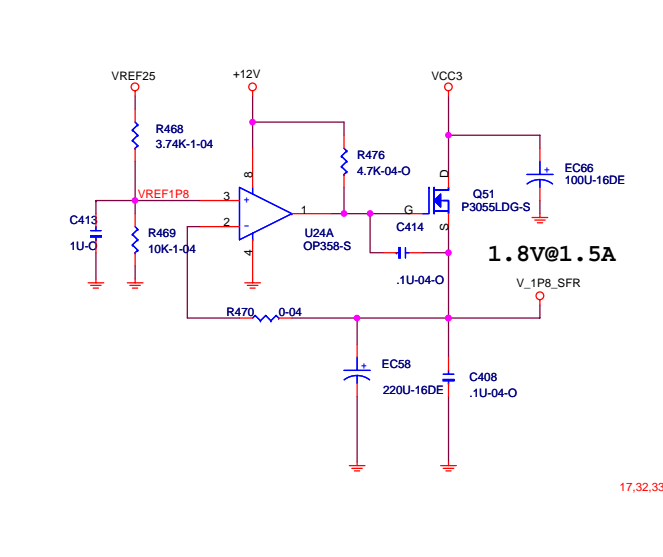




## VDIMM

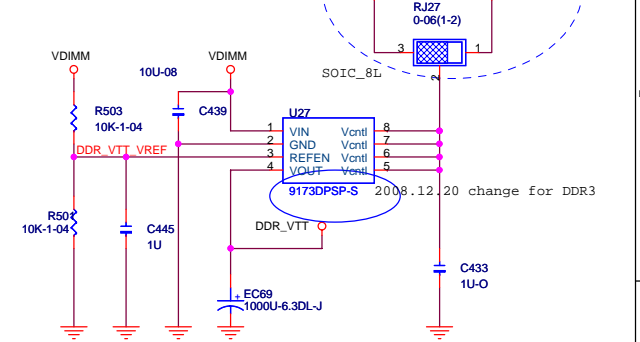


## V\_1P8\_SFR

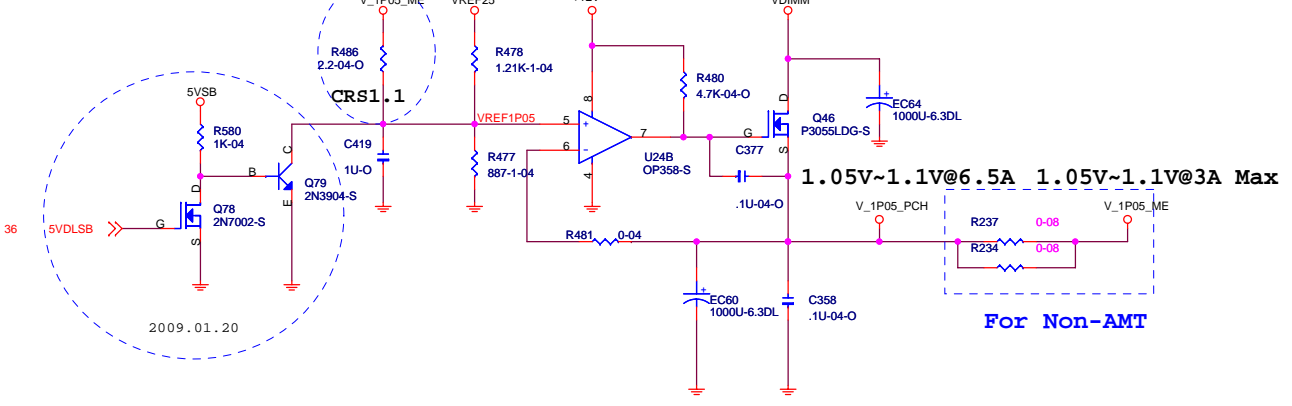


## DDR\_VTT

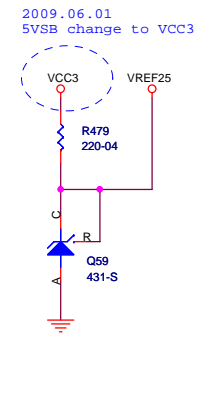
DDR VTT=0.83A (DDR3)



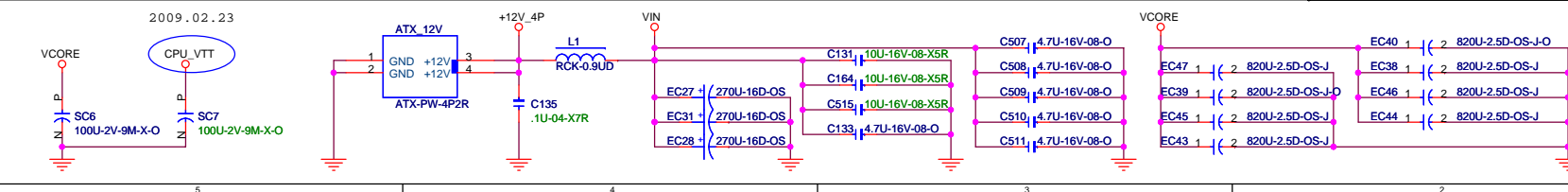
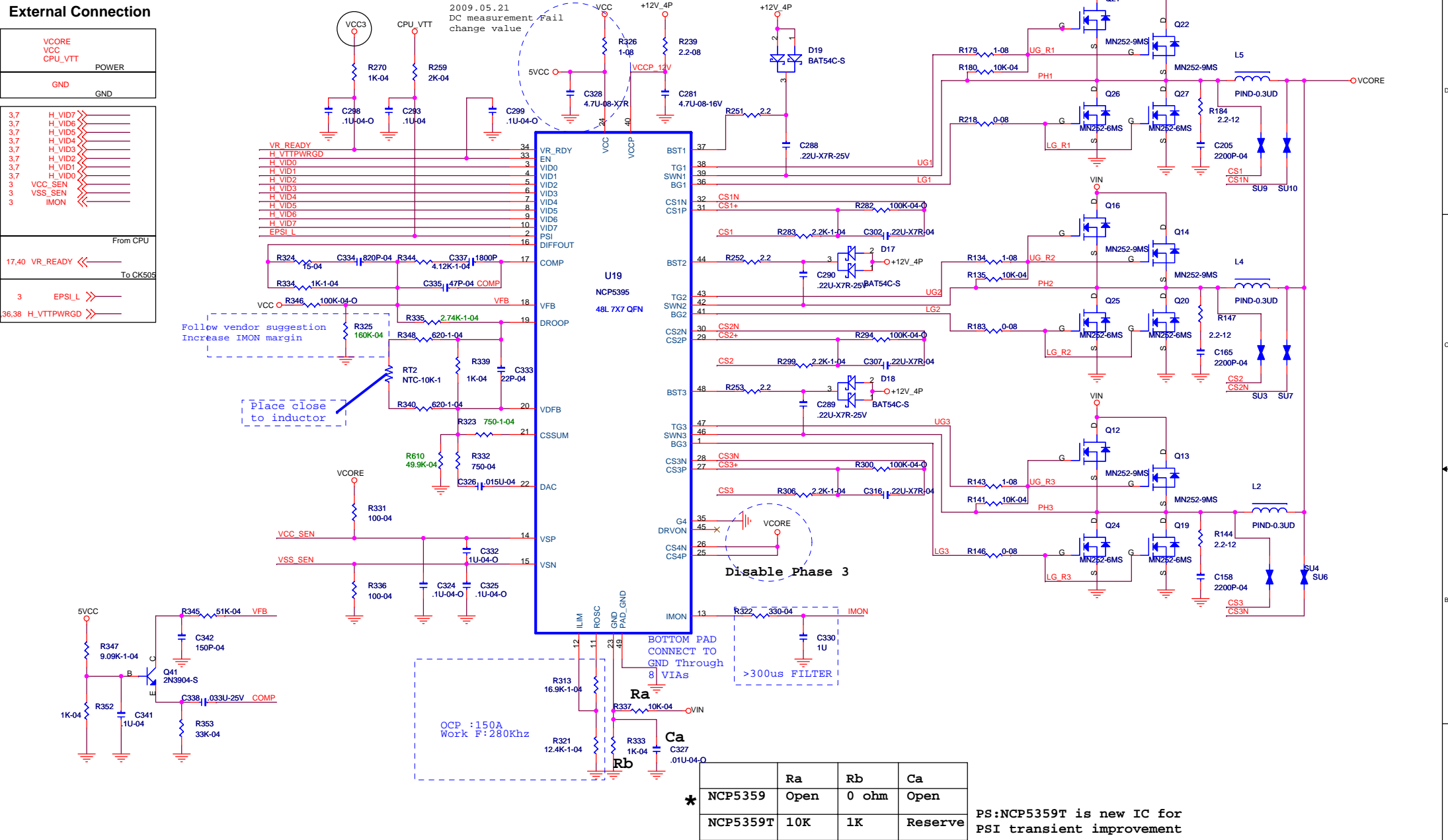
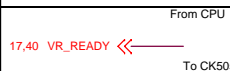
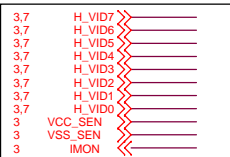
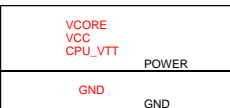
## V\_1P05\_PCH



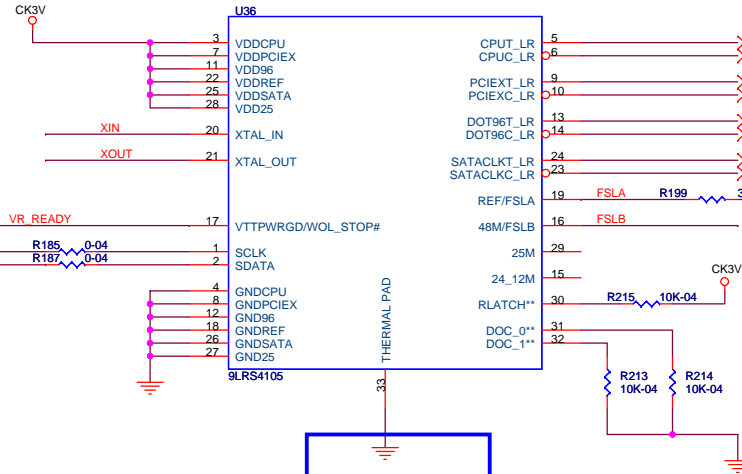
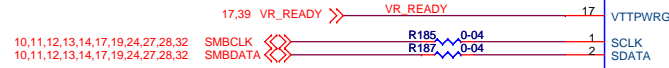
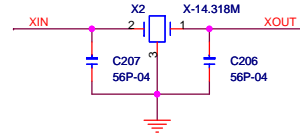
## VREF25



## External Connection



The C206/C207 value depend on CL of X2 crystal  
if CL=20pf C206/C207=33pf  
if CL=32pf C206/C207=56pf

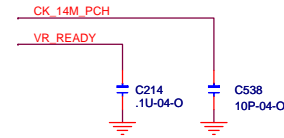
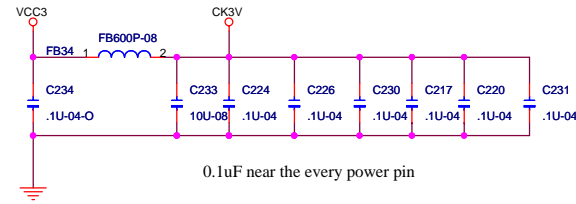
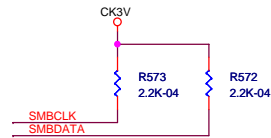


BOTTOM PAD  
CONNECT TO GND  
Through 8 VIAs



FSLB,FSLA = 01, CPU\_CLK = 133MHz

Bit1 FSLB	Bit0 FSLA	CPU CLOCK (MHZ)
0	0	266.66
0	1	133.33
1	0	200.00
1	1	166.66





ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

ATX4P1
12V +/-5%

